RV32M1

72 MHz ARM® Cortex®-M0+/M4F RISC-V RI5CY/ZERO RISCY Quad Core Microcontroller with up to 1280 KB Flash and 384 KB SRAM

The RV32M1 is an ultra-low-power, quad core solution ideal for applications that require a high performance Cortex-M4F/RI5CY processor to run the application and an efficient Cortex-M0+/ ZERO-RISCY to run radio and connectivity stack operations. Applications include portable health care devices, wearable sports and fitness devices, appliances, access control, climate control, energy management, lighting, safety and security systems .

RV32M1

176 VFBGA
9 x 9 x 1 mm Pitch 0.5 mm

Core Processor

- ARM® Cortex®-M4F/RISC-V RI5CY core up to 48 MHz (high-speed run up to 72 MHz) for application code
- ARM® Cortex®-M0+/RISC-V ZERO-RISCY core up to 48 MHz (high-speed run up to 72 MHz) for connectivity stacks

Memories

- 1.25 MB program flash memory, 1 MB on the M4F domain and 256 KB on the M0+ domain
- 384 KB SRAM, 256 KB on the M4F domain and 128 KB on the M0+ domain
- 48 KB ROM with built-in bootloader
- 32 B system register file and 32 B RTC register file
- External bus interface (FlexBUS) for off-chip memory expansion

Clocks

- Low-Power Frequency-Locked Loop (LPFLL)
  - Range 1: 48 MHz
  - Range 2: 72 MHz
- Internal Resistance-Capacitance Oscillators (IRCs)
  - Fast-Speed IRC (48, 52, 56, 60 MHz)
  - Slow-Speed IRC (8 MHz or 2 MHz)
  - Low Power Oscillator (LPO - 1 kHz)
- Real Time Clock Oscillator (RTCOSC)
- System Clock Generation
- Radio Oscillator - 26 or 32 MHz crystal oscillator

System

- Dual Direct Memory Access (DMA) controllers with asynchronous capability

Timers

- 2 x 6 ch., 2 x 2 ch. Timer PWM Modules (TPM)
- 2 x 4 ch. Low Power Programmable Interrupt Timer (LPIT)
- 3 Low Power Timer (LPTMR)
- Real Time Clock (RTC)
- One 56-bit Time stamp

Security and Integrity

- 80-bit unique identification number per chip
- 40-bit unique MAC address field for link layers
- Advanced Flash security and access control
- 16-bit or 32-bit Hardware CRC with programmable generator polynomial
- Low-power Cryptographic Acceleration Unit (CAU3) supporting AES128/196/256, DES/ 3DES, SHA 256, RSA and ECC PK-256/ Curve25519
- True Random Number Generator
- Up to 4 active anti-tamper detection pins

Analog

- 1 x 12-bit single ended low-power ADC
- 2 x Low power comparator (LPCMP) each containing a 6-bit DAC and programmable reference input
- 1 x 12-bit low power digital-to-analog converter (LPDAC)
- 1 x 1.2V/2.1V dual-range VREF

Peripherals

    - M4F: 16 channels, 64 inputs per channel
    - M0+: 8 channels, 32 inputs per channel
- Two internal Watchdog and one external Watchdog Monitor
- Low-leakage wakeup unit
- JTAG and Serial Wire Debug, version 2.0, programming and debug interface with multi-drop capability
- Trace Features for M4F
    - Cross Trigger Interface
    - Embedded Trace Macrocell
    - Trace Port Interface Unit
- Trace Features for M0+
    - Cross Trigger Interface
    - Micro Trace Buffer
    - Breakpoint and Watchpoint Unit
- Nested Vectored Interrupt Controller
- Memory Protection Unit
- Extended Resource Domain Controller

Multi-Standard Radio

- 2.4 GHz Bluetooth Low Energy version 5.0 compliant with support for up to 8 connections
- IEEE Standard 802.15.4 compliant
- Generic FSK modulation
    - GFSK mode supports up to 2000 kbps
    - Modulations: GFSK BT = 0.3, 0.5, 0.7; FSK/MSK
    - Modulation Index: 0.32, 0.5, 0.7 or 1.0
- Typical Receiver Sensitivity (BLE) = -96 dBm
- Typical Receiver Sensitivity (802.15.4) = -100 dBm
- Typical Receiver Sensitivity (250 kbps GFSK-BT=0.5, h=0.5) = -99 dBm
- Programmable Transmitter Output Power: -30 dBm to 3.5 dBm
- Wake-on-Radio allows MCU to sleep longer by processing packets in radio
- Low external component counts for low cost application
- On-chip balun with single ended bidirectional RF port

- 1 x Universal Serial Bus (USB) 2.0 Full Speed (FS) controller with integrated hardware transceiver, 5 V regulator and 2 KB USB RAM
- 1 x 32 ch. FlexIO supporting emulation of UART, I2C, SPI, I2S, Camera IF, LCD RGB, PWM/Waveform generation
- 4 x low power UART (LPUART)
- 4 x low power I2C (LPI2C) modules supporting up to 1 Mbps
- 4 x 16-bit low power SPI (LPSPI) supporting up to 24 Mbps
- 1 x EMVSIM module supporting supporting ISO-7816 protocol
- 1 x Serial Audio Interface (SAI) with support for I2S and AC'97
- 1 x Secure Digital Hardware Controller (uSDHC)

I/O

- 104 General-purpose input/output pins (GPIO)

Power Management

- Bypass mode: 1.71 V to 3.6 V
- Buck DC-DC converter: 2.1 V to 3.6 V
- Core voltage bypass: 1.14 V to 1.45 V direct supply to core, bypassing internal regulator
- Independent VDDIO1 and VDDIO2 supply: 1.71 V to 3.6 V
- Independent VBAT(RTC): 1.71 V to 3.6 V

Packages

- 176 VFBGA 9mm x 9mm x 0.86mm, 0.5mm pitch, -40 °C to 105 °C

Related resources

Type	Description
Selector Guide	The NXP Solution Advisor is a web-based tool that features interactive application wizards and a dynamic product selector.
Reference Manual	The Reference Manual contains a comprehensive description of the structure and function (operation) of a device.
Data Sheet	The Data Sheet includes electrical characteristics and signal connections.
Chip Errata	The chip mask set Errata provides additional or corrective information for a particular device mask set.
Package drawing	Package dimensions are provided in package drawings.

Table of Contents

1 Ordering information

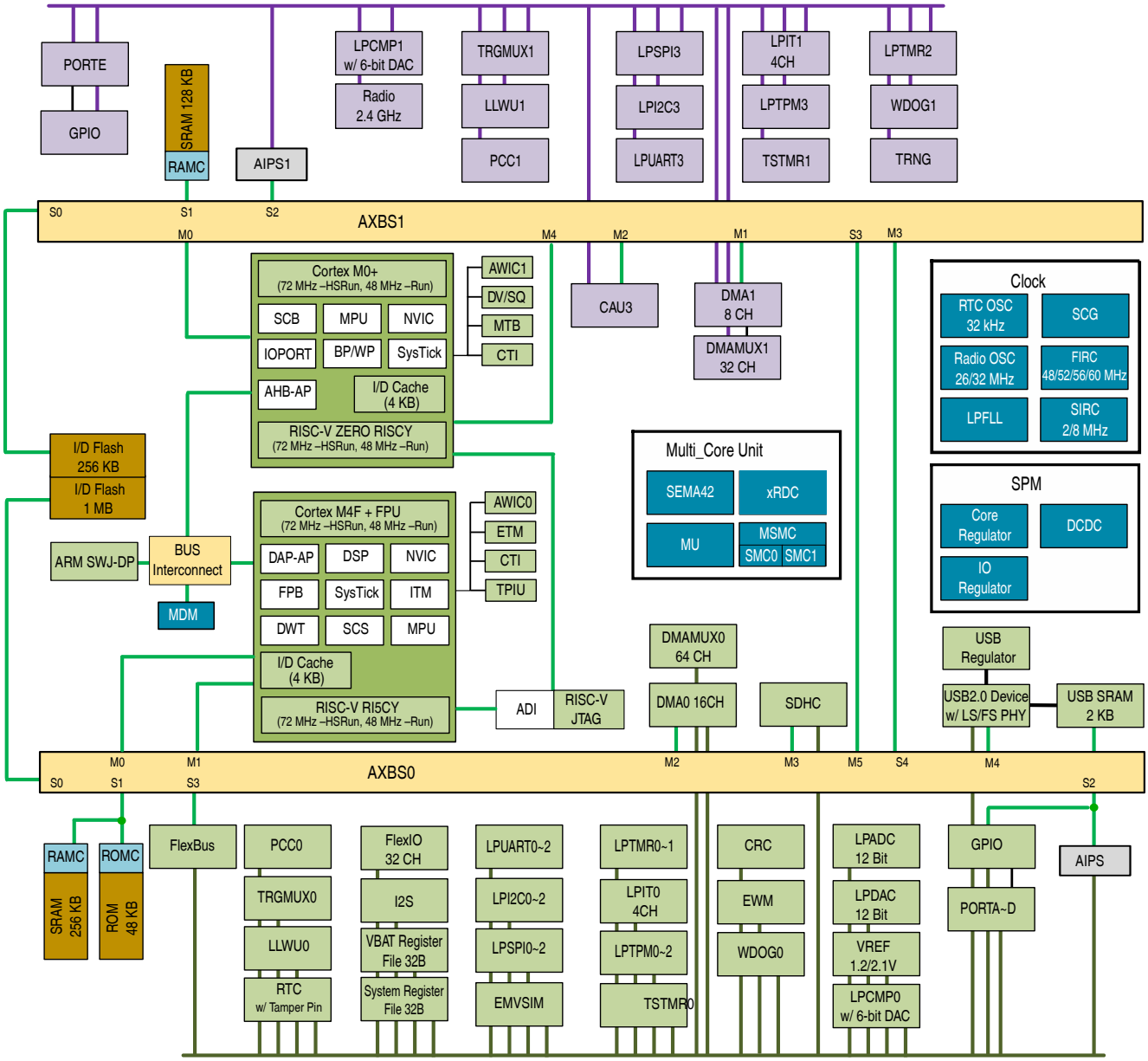
The following table summarizes the part numbers of the devices covered by this document.

Table 1. Ordering information

Product		Memory		Radio			Package	
Part Number	Marking	Flash (MB)	SRAM (KB)	BLE	GENFSK	802.15.4	Pin Count	Package
RV32M1	RV32M1	1.25	384	Yes	Yes	Yes	176	VFBGA

2 Overview

The following figure shows the system diagram of this device



Note: When a core needs access the other AXBS domain resources, the corresponding MUx_CCR[CLKE] bit must be set. AXBS keeps active even if another core enters low power mode (and CPO).

Figure 1. System diagram

The crossbar switch connects bus masters and slaves using a crossbar switch structure. This structure allows up to four bus masters to access different bus slaves simultaneously for AXBS1 and up to six for AXBS0, while providing arbitration among the bus masters when they access the same slave.

2.1 System features

The following sections describe the high-level system features.

2.1.1 ARM Cortex-M0+ core

The enhanced ARM Cortex M0+ is the member of the Cortex-M series of processors targeting microcontroller cores focused on very cost sensitive, low power applications. It has a single 32-bit AMBA AHB-Lite interface and includes an NVIC component. It also has hardware debug functionality including support for simple program trace capability. The processor supports the ARMv6-M instruction set (Thumb) architecture including all but three 16-bit Thumb opcodes (52 total) plus seven 32-bit instructions. It is upward compatible with other Cortex-M profile processors.

This device supports hardware divider (MMDVSQ) when CM0+ core is working.

2.1.2 ARM Cortex-M4 core

The Cortex M4 processor is based on the ARMv7 Architecture and Thumb®-2 ISA and is upward compatible with the Cortex M3, Cortex M1, and Cortex M0 architectures. Cortex M4 improvements include an ARMv7 Thumb-2 DSP (ported from the ARMv7-A/R profile architectures) providing 32-bit instructions with SIMD (single instruction multiple data) DSP style multiply-accumulates and saturating arithmetic.

2.1.3 RISC-V ZERO-RISCY core

ZERO-RISCY is a 2-stage in-order 32b RISC-V processor core. ZERO-RISCY has been designed to be small and efficient.

2.1.4 RISC-V RI5CY core

RI5CY is a 4-stage in-order 32b RISC-V processor core. The ISA of RI5CY was extended to support multiple additional instructions including hardware loops, postincrement load and store instructions and additional ALU instructions that are not part of the standard RISC-V ISA.

2.1.5 NVIC

The ARMv7-M exception model and nested-vectored interrupt controller (NVIC) implement a relocatable vector table supporting many external interrupts, a single non-maskable interrupt (NMI), and priority levels.

The NVIC replaces shadow registers with equivalent system and simplified programmability. The NVIC contains the address of the function to execute for a particular handler. The address is fetched via the instruction port allowing parallel register stacking and look-up. The first sixteen entries are allocated to ARM internal sources with the others mapping to MCU-defined interrupts.

2.1.6 AWIC

The primary function of the Asynchronous Wake-up Interrupt Controller (AWIC) is to detect asynchronous wake-up events in stop modes and signal to clock control logic to resume system clocking. After clock restart, the NVIC observes the pending interrupt and performs the normal interrupt or event processing.

The device uses the following internal and external inputs to the AWIC module. AWIC0 is AWIC in CM4F domain while AWIC1 is AWIC in CM0+ domain.

Table 2. AWIC0 Stop and VLPS wakeup sources

Wake-up source	Description
System resets	All available system resets sources are describted in SMC0 under MSMC chapter
SPM	All available interrupt in SPM, such as low/high voltage detect interrupt, low voltage detect/warnning interrupt, and etc.
Pin	PTA, PTB, PTC, PTD, PTE pin interrupts
LPUART0~3	Functional when using clock source which is active in Stop and VLPS modes
LPI2C0~3	Address match wakeup
LPSPI0~3	Slave mode interrupt
I2S	Functional when using an external bit clock or external master clock
EMVSIM	Any enabled interrupt can be a source as long as the module remains clocked.
USB Controller	Wakeup
Secure Digital Hardware Controller (SDHC)	Wakeup

Table continues on the next page...

Table 2. AWIC0 Stop and VLPS wakeup sources (continued)

Wake-up source	Description
FlexIO	Functional when using clock source which is active in Stop and VLPS modes
LPTMR0~2	Functional when using clock source which is active in Stop, VLPS and LLS/VLLS modes
TPM0~3	Functional when using clock source which is active in Stop and VLPS modes
RTC	Functional in Stop, VLPS, LLS and VLLSx modes
LPIT0/1	Any enabled interrupt can be a source as long as the module remains clocked.
Tamper detect	Interrupt
NMI	NMI is routed to CM4F or CM0+ automatically, only boot core has NMI
LPCMP0/1	Interrupt in normal or trigger mode
LPDAC	Any enabled interrupt can be a source as long as the module remains clocked.
LPADC	The LPADC is functional when using internal clock source
LLWU0	Any enabled interrupt can be a source as long as the module remains clocked.
MUA	Any enabled interrupt can be a source as long as the module remains clocked.
WDOG0	Watchdog0 Interrupt

Table 3. AWIC1 Stop and VLPS wakeup sources

Wake-up source	Description
System resets	All available system resets sources are describted in SMC1 under MSMC chapter
PortE	PTE pin interrupts
LPUART3	Functional when using clock source which is active in Stop and VLPS modes
LPI2C03	Address match wakeup
LPSPI3	Any enabled interrupt can be a source as long as the module remains clocked.
2.4GHz Radio	RF Programmable Interrupt 0
2.4GHz Radio	RF Programmable Interrupt 1
LPTMR2	Functional when using clock source which is active in Stop, VLPS and LLS/VLLS modes
TPM3	Functional when using clock source which is active in Stop and VLPS modes
RTC	Functional in Stop,VLPS,LLS and VLLSx modes
LPIT1	Any enabled interrupt can be a source as long as the module remains clocked.

Table continues on the next page...

Table 3. AWIC1 Stop and VLPS wakeup sources (continued)

Wake-up source	Description
NMI	NMI is routed to CM4F or CM0+ automatically, only boot core has NMI
LPCMP1	Interrupt in normal or trigger mode
TRNG	TRNG has no stop wakeup capability
LLWU1	Any enabled interrupt can be a source as long as the module remains clocked.
MUB	Any enabled interrupt can be a source as long as the module remains clocked.
WDOG1	Watchdog1 Interrupt
INTMUX0~7	All other wakeup sources availabe in AWIC0 can be selected through INTMUXn. Please refer to the INTMUXn description.

2.1.7 Memory

This device has the following features:

- 384 KB of embedded RAM accessible (read/write) at CPU clock speed with 0 wait states.
- 4 KB of embedded RAM used for flash programming acceleration RAM
- The non-volatile memory is divided into two arrays
  - 2 blocks of program flash, providing 1 MB consisting of 4 KB sectors for CM4
  - 1 block of program flash, providing 256 KB consisting of 2 KB sectors for CM0+

  The primary program flash memory contains an IFR space that stores default protection settings and security information.

  The protection setting can protect 64 regions of the primary program flash memory and 16 regions of the secondary program flash memory from unintended erase or program operations.

  The security circuitry prevents unauthorized access to RAM or flash contents from debug port.

- System register file

  This device contains a 32-byte register file that is powered in all power modes.

Also, it retains contents during low power modes and is reset only during a power-on reset.

- VBAT register file

  This device includes a 32-byte register file. The register file is powered by the VBAT domain and is powered in all modes as long as power is applied to the VBAT supply.

  The VBAT register file is only reset during the VBAT Power-on Reset (PORVBAT) sequence.

2.1.8 Reset and boot

The following table lists all the reset sources supported by this device.

NOTE

In the following table, Y means the specific module, except for the registers, bits or conditions mentioned in the footnote, is reset by the corresponding Reset source. N means the specific module is not reset by the corresponding Reset source.

Table 4. Reset source

Reset sources	Descriptions	Modules								
		SPM	SIM	MSMC	LLWU	Reset pin is negated	RTC[1]	LPTMR	Radio	Others
POR reset	Power-on reset (POR)	Y	Y	Y	Y	Y	N	Y	Y[2]	Y
System reset	Low leakage wakeup (LLWU) reset	N[3]	Y[4]	N	N	Y[5]	N	N	Y[2]	Y[6]
	External pin reset (RESET_b)	N[3]	Y[4]	Y[7]	Y	Y	N	N	Y[2]	Y
	Computer operating properly (COP) watchdog reset	N[3]	Y[4]	Y[7]	Y	Y	N	N	Y[2]	Y
	Stop mode acknowledge error (SACKERR)	N[3]	Y[4]	Y[7]	Y	Y	N	N	Y[2]	Y
	Software reset (SW)	N[3]	Y[4]	Y[7]	Y	Y	N	N	Y[2]	Y
	Lockup reset (LOCKUP)	N[3]	Y[4]	Y[7]	Y	Y	N	N	Y[2]	Y
	MDM DAP system reset	N[3]	Y[4]	Y[7]	Y	Y	N	N	Y[2]	Y
Debug reset	Debug reset	N	Y[4]	Y[7]	Y	Y	N	N	Y[2]	Y

1. The VBAT POR asserts on a VBAT POR reset source. It affects only the modules withinthe VBAT power domain: RTC and VBAT Register File. These modules are not affected by the other reset types.
2. Except when RSIM_SW_CONFIG[BLOCK_SOC_RESETS] = 1 to block most of the SoC system or power on resets.
3. Except SPM_CORESC[ACKISO], SPM_CORESC[VSEL] and SPM_CORESC[VSEL_OFFSET]
4. The SIM_SDID, SIM_RREPCR1, SIM_RREPCR2, SIM_RREPSR1, SIM_RREPSR2, SIM_FCFG2, SIM_UIDH, SIM_UIDM, SIM_UIDL, SIM_RFADDRL, SIM_RFADDRH registers are not affected by the reset to exit from VLLS2 or VLLS3 modes.
5. Only if RESET_b is used to wake from VLLS mode.
6. The FTFE, LPCAC and LPLMEM modules cannot be reset when chip is waken up from VLLS2 or VLLS3 modes by LLWU.
7. Except SMCx_PMCTRL and SMCx_PMSTAT of the MSMC.

The CM0+ core adds support for a programmable Vector Table Offset Register (VTOR) to relocate the exception vector table after reset. This device supports booting from:

- internal flash
- ROM

The Flash Option (FOPT) register in the Flash Memory module (FTFE_FOPT) allows the user to customize the operation of the MCU at boot time. The register contains read-only bits that are loaded from the NVM's option byte in the IFR spaces. Below is boot flow chart for this device.

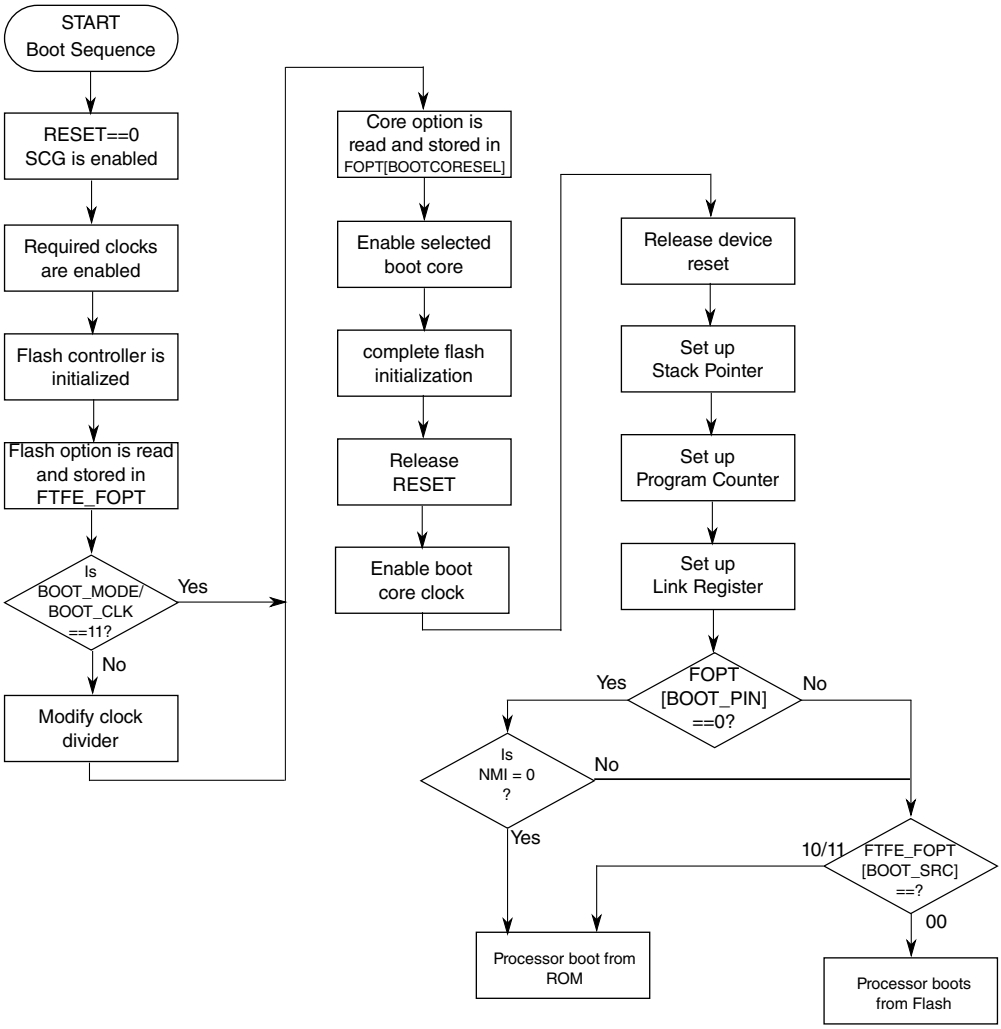


Figure 2. Boot sequence

Blank chips default to boot from ROM and remap the vector table to ROM base address, otherwise, it remaps to flash address.

If booting from ROM, the device executes in boot loader mode.

2.1.9 ROM bootloader

The Kinetis bootloader is the program residing in the on-chip read-only memory (ROM) of a Kinetis microcontroller device. There is hardware logic in place at boot time that either starts execution of an embedded image available on the internal flash memory, or starts the execution of the Kinetis Bootloader from on-chip ROM.

Features supported by the Kinetis Bootloader in Kinetis ROM:

- Supports USB, LPI2C, LPSPI, and LPUART peripheral interfaces

- Automatic detection of the active peripheral
- Ability to disable any peripheral
- LPUART peripheral implements autobaud
- Common packet-based protocol for all peripherals
- Packet error detection and retransmission
- Flash-resident configuration options
- Fully supports internal flash security, including ability to mass erase or unlock security via the backdoor key
- Protection of RAM used by the bootloader while it is running
- Provides command to read properties of the device, such as flash and RAM size
- Multiple options for executing the bootloader either at system start-up or under application control at runtime
- Supports internal flash
- Supports encrypted image download
- ROM boots from either M4 (Default) or M0+ by configuring to FOPT IFR (record Index 0x84)

2.1.10 Clock options

This chip provides a wide range of sources to generate the internal clocks. These sources include internal reference clock (IRC) oscillators, external oscillators, external clock sources, ceramic resonators, and frequency-locked loop (FLL). These sources can be configured to provide the required performance and optimize the power consumption.

The IRC oscillators include the fast internal reference clock (FIRC) oscillator, the slow internal reference clock (SIRC) oscillator, and the low power oscillator (LPO).

The fast internal resistor capacitor (FIRC) oscillator generates a clock ranging between 48 MHz and 60 MHz.

The slow internal resistor capacitor (SIRC) oscillator generates a 8/2 MHz clock. It can serve as the low power, low speed system clock under very low power run (VLPR) mode or very low power wait (VLPW) mode. It can also be provided as clock source for other on-chip modules. The SIRC cannot be used in any VLLS modes.

The LPO generates a 1 kHz clock and default to be off in VLLS0 but can be enabled by configuring bits of SPM_CORELPCNFG[LPOEN] and SPM_CORELPCNFG[ALLREFEN].

The radio oscillator supports high frequency crystals (26 or 32 MHz). It provides clock source not only for RF part but also for other on-chip modules. It serves as the system oscillator as well.

The frequency-locked loop (FLL) can generate a clock with the frequency of 48 MHz or 72 MHz without the need of a reference (a reference clock may only be needed to trim this clock). The FLL can be used as the system clock or clock source for other on-chip modules.

The RTC oscillator supports a low speed crystals (32.768 kHz) and can also support external clock on the EXTAL32 pin for use with the RTC.

For more details on the clock operations and configurations, see Reference Manual.

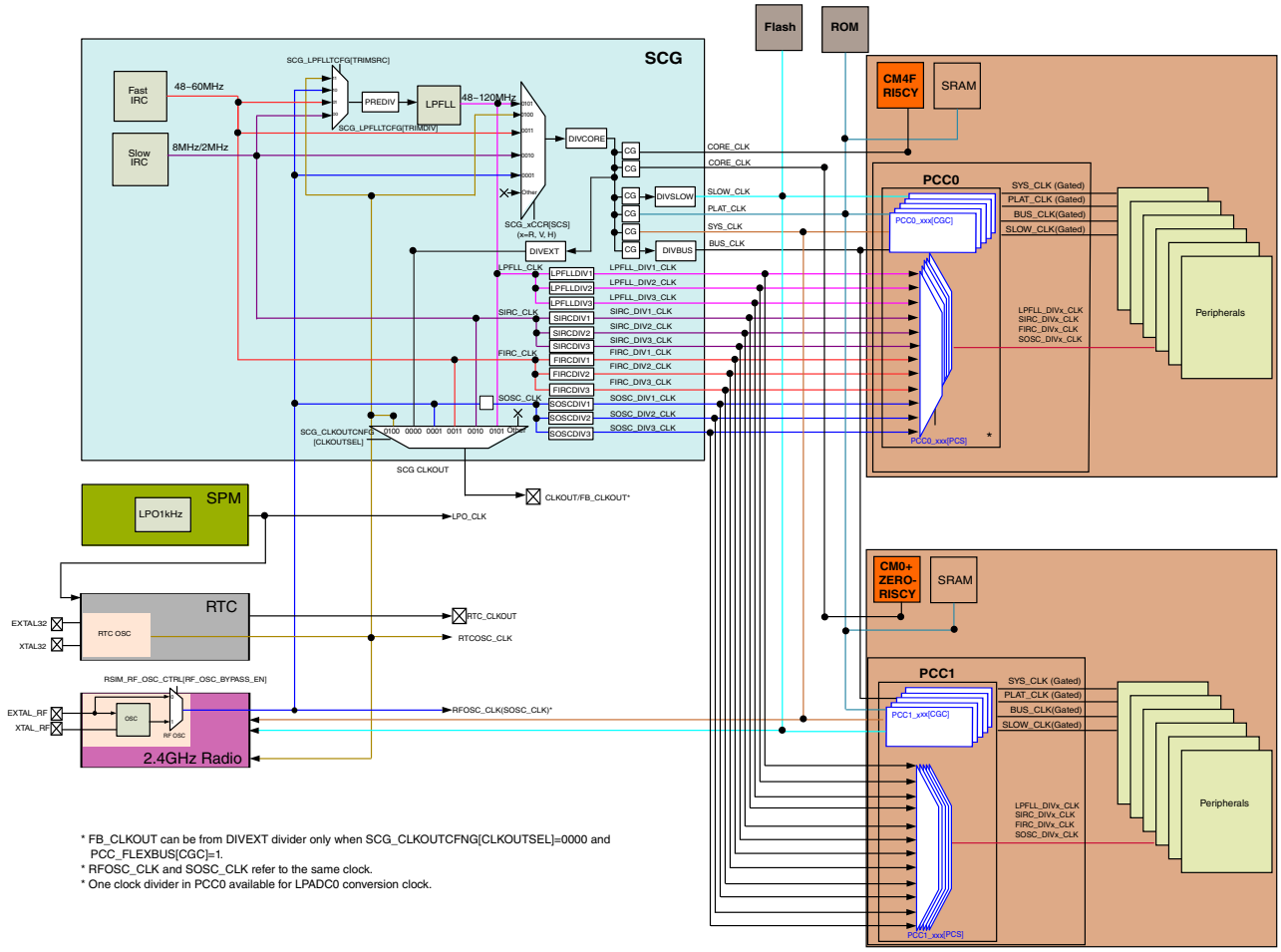


Figure 3. Generic clocking architecture diagram

In order to provide flexibility, many peripherals can select from multiple clock sources for operation. This enables the peripheral to select a clock that will always be available during operation in various operational modes.

The following table summarizes the clocks associated with each module.

Table 5. Clock assignments

Module Name	Bus Interface Clock	PCC Clock Gate	Peripherial Functional Clock	Clock Domain[1]	I/O Interface Clocks
Core Modules					
ARM Cortex-M0+ Core	CORE_CLK	—	—	SCG	—
ARM Cortex-M4 Core	CORE_CLK	—	—	SCG	—
CM0+ TRACE	SYS_CLK	Yes	SYS_CLK	SCG	—
CM4F TRACE	SYS_CLK	Yes	SYS_CLK, SOSC_DIV1_CLK, SIRC_DIV1_CLK, FIRC_DIV1_CLK, LPFLL_DIV1_CLK	PCC0	TRACE_CLK_OUT
JTAG	NA	—	TCK	—	JTAG_TCLK
SWD	PLAT_CLK	—	SWCK	SCG[2]	SWD_CLK
Platform Modules					
CM0+ Crossbar	PLAT_CLK	—	NA	SCG	—
CM4F Crossbar	PLAT_CLK	—	NA	SCG	—
xRDC	PLAT_CLK	Yes	—	PCC0,PCC1	—
SEMA42	PLAT_CLK	Yes	—	PCC0,PCC1	—
System Modules					
MSMC_SMC0	SLOW_CLK	Yes	—	PCC0	—
MSMC_SMC1	SLOW_CLK	Yes	—	PCC1	—
INTMUX	BUS_CLK		—	SCG	—
DMA0	SYS_CLK	Yes	—	PCC0	—
DMA1	SYS_CLK	Yes	—	PCC1	—
DMA MUX0	BUS CLK	Yes	—	PCC0	—
DMA MUX1	BUS CLK	Yes	—	PCC1	—
EWM	SLOW_CLK	Yes	LPO clock.	PCC0[2]	—
LLWU0	SLOW_CLK	Yes	LPO	SCG[2]	—
LLWU1	SLOW_CLK	Yes	LPO	SCG[2]	—
MU	SLOW_CLK	Yes	—	PCC0,PCC1	—
SPM	SLOW_CLK	Yes	—		—
TRGMUX0	SLOW_CLK	Yes	—	SCG	—
TRGMUX1	SLOW_CLK	Yes	—	SCG	—
WDOG0	SLOW_CLK	Yes	RFOSC, LIRC, or LPO clock.	PCC0[2]	—
WDOG1	SLOW_CLK	Yes	RFOSC, LIRC, or LPO clock.	PCC1[2]	—
Memories					

Table continues on the next page...

Table 5. Clock assignments (continued)

Module Name	Bus Interface Clock	PCC Clock Gate	Peripherial Functional Clock	Clock Domain[1]	I/O Interface Clocks
Flash Controller (FMC)	PLAT_CLK	—	—	SCG	—
Flash Memory (FTFE)	SLOW_CLK	—	—	SCG	—
FlexBus	PLAT_CLK	Yes	—	PCC0[2]	FB_CLKOUT/ CLKOUT
CM4F SRAM	PLAT_CLK	—	PLAT_CLK	SCG	—
CM0+ SRAM	PLAT_CLK	—	PLAT_CLK	SCG	—
Security and Integrity					
CAU3	SYS_CLK	Yes	—	PCC1	—
CRC	BUS_CLK	Yes	—	PCC0	—
TRNG	BUS_CLK	Yes	—	PCC1	—
Timers					
LPIT0	SLOW_CLK	Yes	SOSC_DIV3_CLK, SIRC_DIV3_CLK, FIRC_DIV3_CLK, LPFLL_DIV3_CLK	PCC0	—
LPIT1	SLOW_CLK	Yes	SOSC_DIV3_CLK, SIRC_DIV3_CLK, FIRC_DIV3_CLK, LPFLL_DIV3_CLK	PCC1	—
RTC	SLOW_CLK	Yes	RTCOSC, LPO	SCG[2]	RTC_CLKOUT
LPTMR0/1	SLOW_CLK	—	SIRC_DIV3_CLK,LPO, RTCOSC, RFOSC	SCG[2]	—
LPTMR2	SLOW_CLK	—	SIRC_DIV3_CLK,LPO, RTCOSC, RFOSC	SCG[2]	—
LPTPM0~2	BUS_CLK	Yes	SOSC_DIV2_CLK, SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK	PCC0[2]	TPM0~32_CLKIN
LPTPM3	BUS_CLK	Yes	SOSC_DIV2_CLK, SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK	PCC1[2]	TPM3_CLKIN
TSTMR	SLOW_CLK	Auto	SIRC_1MHZ_CLK	SCG	—
Communication Interfaces					
EMVSIM	BUS_CLK	Yes	SOSC_DIV2_CLK, SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK, RTCOSC	PCC0	EMVSIM_CLK

Table continues on the next page...

Table 5. Clock assignments (continued)

Module Name	Bus Interface Clock	PCC Clock Gate	Peripherial Functional Clock	Clock Domain[1]	I/O Interface Clocks
FlexIO	BUS_CLK	Yes	SOSC_DIV2_CLK, SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK	PCC0	—
LPI2C0~2	BUS_CLK	Yes	SOSC_DIV2_CLK, SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK	PCC0	LPI2C0~2_SCL
LPI2C3	BUS_CLK	Yes	SOSC_DIV2_CLK, SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK	PCC1	LPI2C3_SCL
RF Analog	—	—	RFOSC	SCG[2]	RF_BSM_CLK
RF RSIM	SLOW_CLK	—	RTC OSC	SCG[2]	RF_BSM_CLK
RF XCVR	SYS_CLK	—	RFOSC	SCG[2]	RF_BSM_CLK
RF Bluetooth Link Layer	SYS_CLK	—	RTC OSC/RFOSC	SCG[2]	RF_BSM_CLK
RF Generic Link Layer	SYS_CLK	—	RFOSC	SCG[2]	RF_BSM_CLK
RF IEEE 802.15.4 Link Layer	SYS_CLK	—	RFOSC	SCG[2]	RF_BSM_CLK
I2S	BUS_CLK	Yes	SOSC_DIV2_CLK, SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK, SAI_MCLK	PCC0[3]	SAI_TX_BCLK, SAI_RX_BCLK, SAI_MCLK
uSDHC	SYS_CLK	Yes	SOSC_DIV1_CLK, SIRC_DIV1_CLK, FIRC_DIV1_CLK, LPFLL_DIV1_CLK, SDHC_DCLK	PCC0	SDHC_DCLK
LPSPI0~2	BUS_CLK	Yes	SOSC_DIV2_CLK, SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK	PCC0	LPSPI0~2_SCK
LPSPI3	BUS_CLK	Yes	SOSC_DIV2_CLK, SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK	PCC1	LPSPI3_SCK
LPUART0~2	BUS_CLK	Yes	SOSC_DIV2_CLK, SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK	PCC0	—
LPUART3	BUS_CLK	Yes	SOSC_DIV2_CLK, SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK	PCC1	—

Table continues on the next page...

Table 5. Clock assignments (continued)

Module Name	Bus Interface Clock	PCC Clock Gate	Peripherial Functional Clock	Clock Domain[1]	I/O Interface Clocks
USB	SYS_CLK	Yes	SOSC_DIV1_CLK, SIRC_DIV1_CLK, FIRC_DIV1_CLK, LPFLL_DIV1_CLK add note on IRC48	PCC0[2]	—
USB SRAM	SOSC_DIV1_CLK, SIRC_DIV1_CLK, FIRC_DIV1_CLK, LPFLL_DIV1_CLK, SYS_CLK	Yes	—	PCC0[2]	—
Human-Machine Interfaces					
PORTA~D	SLOW_CLK	Yes	SLOW_CLK, LPO	PCC0	—
PORTE	SLOW_CLK	Yes	SLOW_CLK, LPO	PCC1	—
RGPIOA~D	PLAT_CLK	Yes	—	PCC0	—
RGPIOE	PLAT_CLK	Yes	—	PCC1	—
Analog					
LPADC	BUS_CLK	Yes	SOSC_DIV2_CLK, SIRC_DIV2_CLK, FIRC_DIV2_CLK, LPFLL_DIV2_CLK, LPADC Internal Clock.	PCC0	—
LPCMP0	SLOW_CLK	—	—	SCG	—
LPCMP1	SLOW_CLK	—	—	SCG	—
LPDAC	BUS_CLK	Yes	—	PCC0	—
VREF	SLOW_CLK	Yes	—	PCC0	—

1. PPC0 controls CM4F domain,and PPC1 controls CM0+ domain.
2. It is bus interface clock domain.
3. SAI_MCLK doesn't blong to PCC clock domain.

2.1.11 Security

Security state can be enabled via programming Flash IFR SEC0 (index 0x80). After enabling device security, the SWJ (SWD and JTAG) port cannot access the memory resources of the MCU, and ROM boot loader is also limited to access flash and not allowed to read out flash information via ROM boot loader commands.

Access interface	Secure state	Unsecure operation
SWJ (SWD and JTAG) port	Cannot access memory source by SWD interface	The debugger can write 1 to the System Reset Request field and Flash Mass Erase in Progress field of the

Table continues on the next page...

Access interface	Secure state	Unsecure operation
		MDM-AP Control register to trigger a mass erase (Erase All Blocks Unsecure) command
ROM boot loader Interface (LPUART/ LPI2C/LPSPI/USB)	Limit access to the flash, cannot read out flash content	Send “FlashEraseAllUnsecure" command or attempt to unlock flash security using the backdoor key

This device features 80-bit unique identification number, which is programmed in factory and loaded to SIM register after power-on reset.

2.1.12 Power management

These devices include on-chip LDO regulators and an on-chip DCDC converter to condition the main power supply voltage and allow for flexibility in power configurations. Three operating modes are supported: Bypass, LDO only, and DCDC (buck mode).

The SPM provides Stop (STOP), Very Low Power Stop (VLPS), Low Leakage Stop (LLS), and Very Low Leakage Stop (VLLS) configurations in ARM®’s Deep Sleep operational mode. In these modes, the MCU core and most of the peripherals are disabled. Depending on the requirements of the application, different portions of the analog, logic, and memory can be retained or disabled to conserve power.

The Nested Vectored Interrupt Controller (NVIC), the Asynchronous Wake-up Interrupt Controller (AWIC), and the Low Leakage Wake-Up Controller (LLWU) are used to wake up the MCU from low power states. The NVIC is used to wake up the MCU core from WAIT and VLPW modes. The AWIC is used to wake up the MCU core from STOP and VLPS modes. The LLWU is used to wake up the MCU core from LLS and VLLS modes.

For additional information regarding operational modes, power management, the NVIC, AWIC, or the LLWU, please refer to the Reference Manual.

The following table shows module operations in different low power modes:

Table 7. Module operation in low power modes

Modules	VLPR	VLPW	STOP	VLPS	LLS	VLLS2/3	VLLS0/1
Core modules							
NVIC	FF	FF	SR	SR	SR	OFF	OFF
System modules							

Table continues on the next page...

Table 7. Module operation in low power modes (continued)

Modules	VLPR	VLPW	STOP	VLPS	LLS	VLLS2/3	VLLS0/1
MSMC	FF	FF	FF	FF	SR/FF[1]	OFF/FF[2]	OFF/FF[2]
LLWUx	FF	FF	FF	FF	FF	FF	FF
Core regulator (1.2 V)	Optional[3]	Optional[3]	Optional[3]	Optional[3]	Optional[3]	Optional[3]	Optional[3]
IOREG 1.8 V	Optional[3]	Optional[3]	Optional[3]	Optional[3]	Optional[3]	Optional[3]	Optional[3]
HVD/LVD	Optional[4]	Optional[4]	Optional[4]	Optional[4]	Optional[4]	Optional[4]	Optional[4]
POR (Brown-Out)	FF	FF	FF	FF	FF	FF	Optional[5]
DMA	FF	FF	Async	Async	SR	OFF	OFF
Watchdog	FF	FF	Optional on with available clock source	Optional on with available clock source	SR	OFF	OFF
Clocks							
1 kHz LPO	FF	FF	FF	FF	FF	FF	Optional[6]
Radio OSC	Optional[7]	Optional[7]	Optional[7]	Optional[7]	Optional[7]	Optional[7]	Optional[7]
SCG	8 MHz SIRC	8 MHz SIRC	static – SIRC, FIRC, LPFLL optional	static – SIRC optional	static	OFF	OFF
Core clock	FF	OFF	OFF	OFF	OFF	OFF	OFF
Plat clock	FF	FF	OFF	OFF	OFF	OFF	OFF
Bus clock	FF	FF	OFF	OFF	OFF	OFF	OFF
Slow clock	FF	FF	OFF	OFF	OFF	OFF	OFF
Memory							
Flash	1 MHz No program	LP	LP	LP	SR	The registers are retained	OFF
SRAM	LP	LP	SR	Optional[8]	Optional[8]	Optional[8]	OFF
LPLMEM (Cache)	FF	FF	SR	SR	Optional retention	Optional[8]	OFF
LPCAC (Cache)	FF	FF	SR	SR	Optional retention	Optional[8]	OFF
System Register File	FF	FF	FF	FF	FF	FF	FF
VBAT Register File	Optional[9]	Optional[9]	Optional[9]	Optional[9]	Optional[9]	Optional[9]	Optional[9]
Communication Interface							
USB	static	static	static	static	static	OFF	OFF
USB Reg	Optional	Optional	Optional	Optional	Optional	Optional	Optional
LPUARTx	1 Mbit/s	1 Mbit/s	Async	Async	static	OFF	OFF
LPSPIx	Master 2 Mbit/s Slave 1 Mbit/s	Master 2 Mbit/s Slave 1 Mbit/s	Static, slave mode receive	Static, slave mode receive	static	OFF	OFF

Table continues on the next page...

Table 7. Module operation in low power modes (continued)

Modules	VLPR	VLPW	STOP	VLPS	LLS	VLLS2/3	VLLS0/1
LPI2Cx	1 Mbit/s	1 Mbit/s	Async	Async	static	OFF	OFF
I2S	FF	FF	Async	Async	static	OFF	OFF
EMVSIM	FF	FF	Static, card detect wakeup	Static, card detect wakeup	static	OFF	OFF
Timer modules							
LPTPMx	FF	FF	Async	Async	static	OFF	OFF
LPIT	FF	FF	Async	Async	static	OFF	OFF
LPTMRx	FF	FF	Async	Async	Async	FF	FF
RTC	FF	FF	Async	Async	Async	Optional[9]	Optional[9]
TSTMR	FF	FF	static	static	static	OFF	OFF
Security modules							
CAU3	FF	FF	static	static	static	OFF	OFF
CRC	FF	FF	static	static	static	OFF	OFF
Digital Tamper	FF	FF	Async	Async	Async	Optional[9]	Optional[9]
TRNG	FF	FF	static	static	static	OFF	OFF
Analog							
LPADC	FF	FF	LPADC internal clock	LPADC internal clock	SR	OFF	OFF
LPCMP0	FF	FF	FF	FF or Low power Nano mode Compare	FF or Low power Nano mode Compare	FF	FF[10]
LPCMP1	FF	FF	FF	FF or Low power Nano mode Compare	FF or Low power Nano mode Compare	Optional[11]	Optional[11]
6-bit DAC	FF	FF	static	static	static	OFF	OFF
12-bit LPDAC	FF	FF	static	static	static	OFF	OFF
VREF	FF	FF	static	static	static	OFF	OFF
HMI							
GPIO	FF	FF	Static output, wake up input	Static output, wake up input	Static, pins latched	OFF, pins latched	OFF, pins latched
FlexIO	FF	FF	Async	Async	SR	OFF	OFF

1. SR for reset related control and FF for power model related control
2. OFF for reset related control and FF for power model related control
3. It depends on MCU/RF arbitration and SPM LPSEL/BGEN bit.
4. It depends on MCU/RF arbitration and SPM LVDEN/BGEN/ALLREFN bit
5. It depends on MCU/RF arbitration and SPM POREN bit.
6. It depends on MCU/RF arbitration and SPM LPOEN/ALLREFN bit.
7. It depends on MCU/RF configuration and arbitration.
8. It depends on the configurations, see the next table for details.
9. Requires the VBAT supply to be properly powered.

10. It depends on SPM_CORELPCNFG[ALLREFEN] =1.
11. It depends on SPM_CORESC[VDDIOOVRIDE] = 1, SPM_CORELPCNFG[ALLREFEN] =1, and VDDIO2.

The following tables list all power mode combinations and corresponding power behaviors.

Table 8. MCU power mode combinations

CM4F power mode[1]	CM0+ power mode[2]	Max CM4F core clock frequency	Max CM0+ core clock frequency	MCU power mode[3]
RUN	RUN	48MHz	48MHz	RUN
RUN	HSRUN	72MHz	72MHz	HSRUN
RUN	VLPR	48MHz	48MHz	RUN
RUN	VLPW	48MHz	OFF	RUN
RUN	VLPS	48MHz	OFF	RUN
RUN	STOP/PSTOP	48MHz	OFF	RUN
RUN	LLS	48MHz	OFF	RUN
RUN	VLLS	48MHz	OFF	RUN
HSRUN	RUN	72MHz	72MHz	HSRUN
HSRUN	HSRUN	72MHz	72MHz	HSRUN
HSRUN	VLPR	72MHz	72MHz	HSRUN
HSRUN	VLPW	72MHz	OFF	HSRUN
HSRUN	VLPS	72MHz	OFF	HSRUN
HSRUN	STOP/PSTOP	72MHz	OFF	HSRUN
HSRUN	LLS	72MHz	OFF	HSRUN
HSRUN	VLLS	72MHz	OFF	HSRUN
VLPR	RUN	48MHz	48MHz	RUN
VLPR	HSRUN	72MHz	72MHz	HSRUN
VLPR	VLPR	8MHz	8MHz	VLP
VLPR	VLPW	8MHz	OFF	VLP
VLPR	VLPS	8MHz	OFF	VLP
VLPR	STOP/PSTOP	48MHz	OFF	RUN
VLPR	LLS	8MHz	OFF	VLP
VLPR	VLLS	8MHz	OFF	VLP
VLPW	RUN	OFF	48MHz	RUN
VLPW	HSRUN	OFF	72MHz	HSRUN
VLPW	VLPR	OFF	8MHz	VLP
VLPW	VLPW	OFF	OFF	VLP
VLPW	VLPS	OFF	OFF	VLP
VLPW	STOP/PSTOP	OFF	OFF	RUN
VLPW	LLS	OFF	OFF	VLP
VLPW	VLLS	OFF	OFF	VLP
VLPS	RUN	OFF	48MHz	RUN

Table continues on the next page...

Table 8. MCU power mode combinations (continued)

CM4F power mode[1]	CM0+ power mode[2]	Max CM4F core clock frequency	Max CM0+ core clock frequency	MCU power mode[3]
VLPS	HSRUN	OFF	72MHz	HSRUN
VLPS	VLPR	OFF	8MHz	VLP
VLPS	VLPW	OFF	OFF	VLP
VLPS	VLPS	OFF	OFF	VLP
VLPS	STOP/PSTOP	OFF	OFF	RUN
VLPS	LLS	OFF	OFF	VLP
VLPS	VLLS	OFF	OFF	VLP
STOP/PSTOP	RUN	OFF	48MHz	RUN
STOP/PSTOP	HSRUN	OFF	72MHz	HSRUN
STOP/PSTOP	VLPR	OFF	8MHz	RUN
STOP/PSTOP	VLPW	OFF	OFF	RUN
STOP/PSTOP	VLPS	OFF	OFF	RUN
STOP/PSTOP	STOP/PSTOP	OFF	OFF	RUN
STOP/PSTOP	LLS	OFF	OFF	RUN
STOP/PSTOP	VLLS	OFF	OFF	RUN
LLS	RUN	OFF	48MHz	RUN
LLS	HSRUN	OFF	72MHz	HSRUN
LLS	VLPR	OFF	8MHz	VLP
LLS	VLPW	OFF	OFF	VLP
LLS	VLPS	OFF	OFF	VLP
LLS	STOP/PSTOP	OFF	OFF	RUN
LLS	LLS	OFF	OFF	LLS
LLS	VLLS	OFF	OFF	LLS
VLLS	RUN	OFF	48MHz	RUN
VLLS	HSRUN	OFF	72MHz	HSRUN
VLLS	VLPR	OFF	8MHz	VLP
VLLS	VLPW	OFF	OFF	VLP
VLLS	VLPS	OFF	OFF	VLP
VLLS	STOP/PSTOP	OFF	OFF	RUN
VLLS	LLS	OFF	OFF	LLS
VLLS	VLLS	OFF	OFF	VLLS

1. It is configured by SMC0_PMCTRL register of MSMC.
2. It is configured by SMC1_PMCTRL register of MSMC.
3. It can be read out from SMCx_PMCSTAT register of MSMC. Please note the PMSTAT[7:0] bits in both SMC0_PMCSTAT and SMC1_PMCSTAT registers refer to MCU power mode so their value are identical. The STOPSTAT[31:24] bits in SMCx_PMCSTAT register reflect separate CM4F or CM0+ clock status, so can be different.

Table 9. System power mode

MCU power mode[1]	RF power mode[2]	System power mode	
		MCU power status	RF power status
RUN	RRUN	RUN	RRUN
RUN	RLLS	RUN	RLLS
RUN	RVLLS	RUN	RVLLS
HSRUN	RRUN	HSRUN	RRUN
HSRUN	RLLS	HSRUN	RLLS
HSRUN	RVLLS	HSRUN	RVLLS
VLP	RRUN	RUN	RRUN
VLP	RLLS	VLP	RLLS
VLP	RVLLS	VLP	RVLLS
LLS	RRUN	LLS	RRUN
LLS	RLLS	LLS	RLLS
LLS	RVLLS	LLS	RVLLS
VLLS	RRUN	VLLS	RRUN
VLLS	RLLS	VLLS	RLLS
VLLS	RVLLS	VLLS	RVLLS

1. It can be read out from SMCx_PMCSTAT register of MSMC. Please note the PMSTAT[7:0] bits in both SMC0_PMCSTAT and SMC1_PMCSTAT registers refer to MCU power mode so their value are identical. The STOPSTAT[31:24] bits in SMCx_PMCSTAT register reflect separate CM4F or CM0+ clock status, so can be different.
2. It is configured by RSIM Power Control register. The user can read out relative bit in this register to determine RF power mode status.

Table 10. Note

FF	Full functionality. In VLPR and VLPW, the system frequency is limited, but if a module does not have a limitation in its functionality, it is still listed as FF.
Async	Fully functional with alternate clock source, provided the selected clock source remains enabled
SR	Module state is retained but not functional.
LP	Module operates in a lower power state.
Off	Module is powered off and in reset state upon wake-up

The following table provides the modules that can wake MCU from low power modes.

Modules	VLPW	STOP	VLPS	LLS	VLLS3	VLLS1	VLLS0
RTC	Y	Y	Y	Y[1]	Y[1]	Y[1]	Y[2]
LPTMRx	Y	Y	Y	Y[1]	Y[1]	Y[1]	Y[3]
LPTPMx	Y	Y	Y	N	N	N	N
LPITx	Y	Y	Y	N	N	N	N

Table continues on the next page...

Modules	VLPW	STOP	VLPS	LLS	VLLS3	VLLS1	VLLS0
LLWUx	Y	Y	Y	Y	Y	Y	Y
LPSPIx	Y	Y	Y	N	N	N	N
LPI2Cx	Y	Y	Y	N	N	N	N
FlexIO	Y	Y	Y	N	N	N	N
LPUARTx	Y	Y	Y	N	N	N	N
USB	Y	Y	N	N	N	N	N
ADC	Y	Y	Y	N	N	N	N
LPCMPx	Y	Y	Y	Y[1]	Y[1]	Y[1]	N
LVD/HVD	Y	Y	Y	Y	Y	Y	Y
GPIO(except NMI,RESET)	Y	Y	Y	Y[4]	Y[4]	Y[4]	Y[4]
NMI	Y	Y	Y	Y	Y	Y	Y
RESET	Y	Y	Y	Y	Y	Y	Y
Radio	Y	Y	Y	Y	Y	Y	Y

1. Need to configure this module as wakeup source of LLWU
2. Need to set EXTAL32 as RTC clock source and configure this module as wakeup source for LLWU
3. LPTMRs use RF OSC, EXTAL32 or LPO in VLLS0.
4. Only that pins available to configure to wakeup source of LLWU

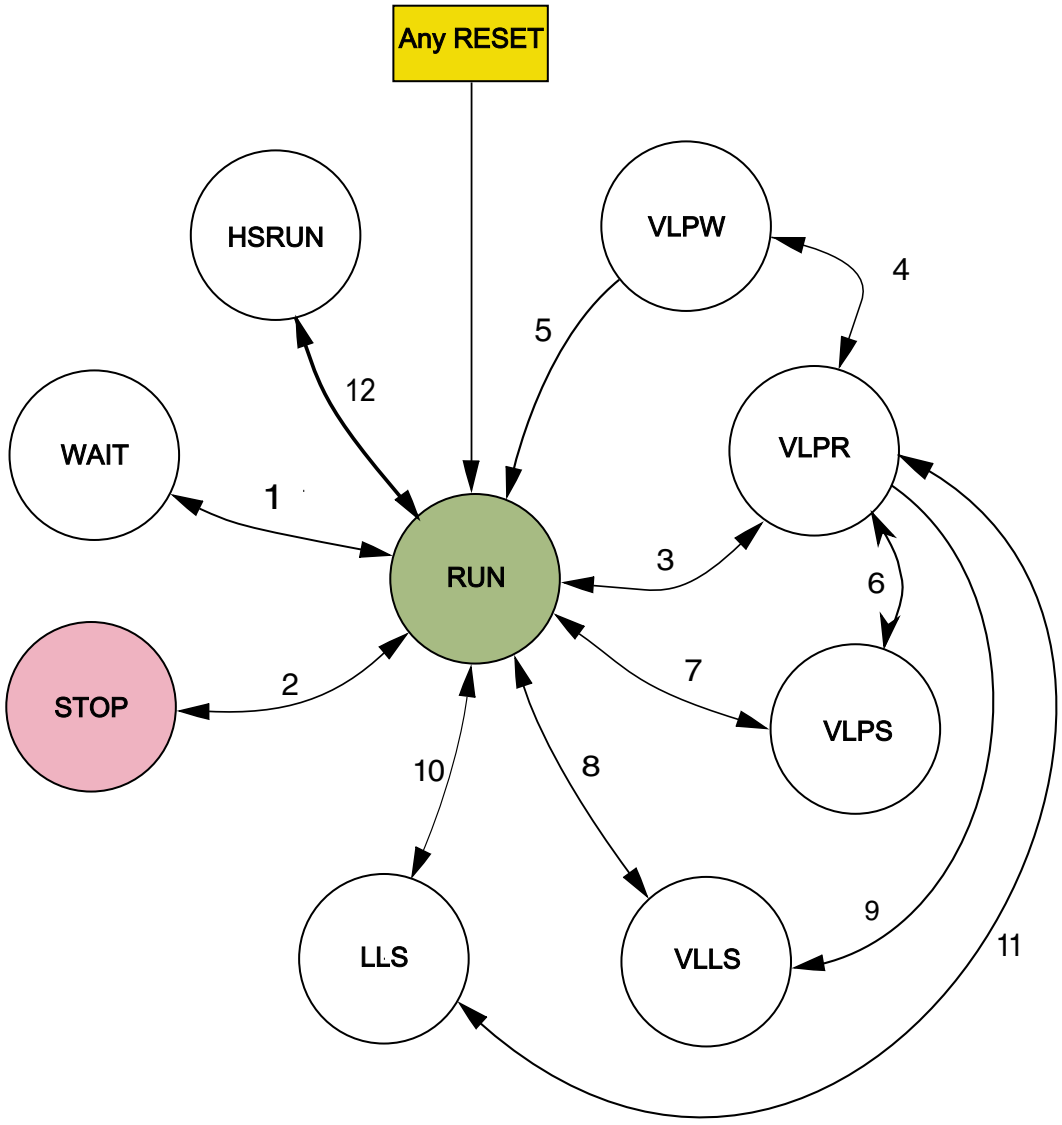


Figure 4. Power mode state transition diagram

2.1.13 LLWU

The LLWU module is used to wake MCU from low leakage power mode (LLS and VLLSx) and functional only on entry into a low-leakage power mode. After recovery from LLS, the LLWU is immediately disabled. After recovery from VLLSx, the LLWU continues to detect wake-up events until the user has acknowledged the wake-up event.

The following is internal peripheral and external pin inputs as wakeup sources for the Coretex-M4 core (CPU0).

Table 12. Wakeup Sources for LLWU0 inputs

LLWU0 pin	Module source or pin name
LLWU_P0	PTA1
LLWU_P1	PTA2
LLWU_P2	PTA22
LLWU_P3	PTA30
LLWU_P4	PTB1
LLWU_P5	PTB2
LLWU_P6	PTB4
LLWU_P7	PTB6
LLWU_P8	PTB7
LLWU_P9	PTB8
LLWU_P10	PTB16
LLWU_P11	PTB20
LLWU_P12	PTB22
LLWU_P13	PTB25
LLWU_P14	PTB28
LLWU_P15	PTC7
LLWU_P16	PTC9
LLWU_P17	PTC11
LLWU_P18	PTC12
LLWU_P19	PTD8
LLWU_P20	PTD10
LLWU_P21	PTE1[1]
LLWU_P22	PTE3[1]
LLWU_P23	PTE8[1]
LLWU_P24	PTE9[1]
LLWU_P25	PTE10[1]
LLWU_P26	PTE12[1]
LLWU_P27	Reserved[2]
LLWU_P28	Reserved[3]
LLWU_P29	USB0 VREGIN
LLWU_P30	USB0_DP[4]
LLWU_P31	USB0_DM[4]
LLWU_M0IF	LPTMR0, LPTMR1, LPTMR2 (sharing M0IF)[5]
LLWU_M1IF	LPCMP0[6]
LLWU_M2IF	LPCMP1[7]
LLWU_M3IF	Reserved[8]
LLWU_M4IF	Reserved[9]
LLWU_M5IF	Tamper Detect[10]

Table continues on the next page...

Table 12. Wakeup Sources for LLWU0 inputs (continued)

LLWU0 pin	Module source or pin name
LLWU_M6IF	RTC Alarm[10]
LLWU_M7IF	RTC Seconds[10]
LLWU_M0DR	LPTMR0 Asynchronous DMA
LLWU_M1DR	LPTMR1 Asynchronous DMA
LLWU_M2DR	LPTMR2 Asynchronous DMA
LLWU_M3DR	Reserved[11]
LLWU_M4DR	LPTMR0 Trigger
LLWU_M5DR	LPTMR1 Trigger
LLWU_M6DR	LPTMR2 Trigger
LLWU_M7DR	Reserved[12]

1. Set SPM_CORESC[VDDIOOVRIDE] for all PTE pins to wakeup from VLLS0/1
2. The corresponding LLWU0_PE[23: 22], LLWU0_PF[27], LLWU0_PDC2[27], and LLWU0_PMC[27] are reserved.
3. The corresponding LLWU0_PE[25: 24], LLWU0_PF[28], LLWU0_PDC2[28], and LLWU0_PMC[28] are reserved.
4. Set SPM_CORESC[USBOVRIDE] to wakeup from VLLS0 or VLLS1.
5. Requires the peripheral and the peripheral interrupt to be enabled. The LLWU's WUME bit enables the internal module flag as a wakeup input. After wakeup, the flags are cleared based on the peripheral clearing mechanism.
6. Set SPM_CORELPCNFG[ALLREFEN] to wakeup from VLLS0/1.
7. Set SPM_CORESC[VDDIOOVRIDE] and SPM_CORELPCNFG[ALLREFEN] to wakeup from VLLS0/1.
8. The corresponding LLWU0_ME[3] is reserved.
9. The corresponding LLWU0_ME[4] is reserved.
10. Set SPM_CORESC[VDDIOOVRIDE] to wakeup from VLLS0 or VLLS1.
11. The corresponding LLWU0_DE[3] is reserved.
12. The corresponding LLWU0_DE[7] is reserved.

The following is internal peripheral and external pin inputs as wakeup sources for the Coretex-M0+ core (CPU1).

Table 13. Wakeup Sources for LLWU1 inputs

LLWU1 pin	Module source or pin name
LLWU_P0	PTA1
LLWU_P1	PTA2
LLWU_P2	PTA22
LLWU_P3	PTA30
LLWU_P4	PTB1
LLWU_P5	PTB2
LLWU_P6	PTB4
LLWU_P7	PTB6
LLWU_P8	PTB7
LLWU_P9	PTB8
LLWU_P10	PTB16
LLWU_P11	PTB20

Table continues on the next page...

Table 13. Wakeup Sources for LLWU1 inputs (continued)

LLWU1 pin	Module source or pin name
LLWU_P12	PTB22
LLWU_P13	PTB25
LLWU_P14	PTB28
LLWU_P15	PTC7
LLWU_P16	PTC9
LLWU_P17	PTC11
LLWU_P18	PTC12
LLWU_P19	PTD8
LLWU_P20	PTD10
LLWU_P21	PTE1
LLWU_P22	PTE3
LLWU_P23	PTE8
LLWU_P24	PTE9
LLWU_P25	PTE10
LLWU_P26	PTE12
LLWU_P27	Reserved[1]
LLWU_P28	Reserved[2]
LLWU_P29	USB0 VREGIN
LLWU_P30	USB0_DP[-1]
LLWU_P31	USB0_DM[-1]
LLWU_M0IF	LPTMR0, LPTMR1, LPTMR2 (sharing M0IF)[3]
LLWU_M1IF	LPCMP0
LLWU_M2IF	LPCMP1
LLWU_M3IF	Wake-From-Radio (WFR)
LLWU_M4IF	Reserved[4]
LLWU_M5IF	Tamper Detect[-1]
LLWU_M6IF	RTC Alarm[-1]
LLWU_M7IF	RTC Seconds[-1]
LLWU_M0DR	LPTMR0 Asynchronous DMA
LLWU_M1DR	LPTMR1 Asynchronous DMA
LLWU_M2DR	LPTMR2 Asynchronous DMA
LLWU_M3DR	Reserved[5]
LLWU_M4DR	LPTMR0 Trigger
LLWU_M5DR	LPTMR1 Trigger
LLWU_M6DR	LPTMR2 Trigger
LLWU_M7DR	Reserved[6]

1. The corresponding LLWU1_PE[23:22], LLWU1_PF[27], LLWU1_PDC2[27], and LLWU1_PMC[27] are reserved.
2. The corresponding LLWU1_PE[25:24], LLWU1_PF[28], LLWU1_PDC2[28], and LLWU1_PMC[28] are reserved.

3. Requires the peripheral and the peripheral interrupt to be enabled. The LLWU's WUME bit enables the internal module flag as a wakeup input. After wakeup, the flags are cleared based on the peripheral clearing mechanism.
4. The corresponding LLWU1_ME[4] is reserved.
5. The corresponding LLWU1_DE[3] is reserved.
6. The corresponding LLWU1_DE[7] is reserved.

2.1.14 Debug controller

This device supports standard ARM 2-pin SWD and JTAG debug port. It provides register and memory accessibility from the external debugger interface, basic run/halt control plus 4 breakpoints and 2 watchpoints.

It also supports trace function with the Micro Trace Buffer (MTB), which provides a simple execution trace capability for the Cortex-M0+ processor.

2.1.15 INTMUX

The Interrupt Multiplexer (INTMUX) routes the interrupt sources to the interrupt outputs. It provides interrupt status registers to monitor interrupt pending status and vector numbers and implements the ability to logical AND or OR enabled interrupts on a given channel.

The INTMUX has the following features:

- Supports 4 multiplex channels
- Each channel receives 32 interrupt sources and has one interrupt output
- Each interrupt source can be enabled or disabled
- Each channel supports logic AND or logic OR of all enabled interrupt sources

2.1.16 FlexBus

The FlexBus multifunction external bus interface controller is a hardware module.

The FlexBus has the following features:

- 6 independent, user-programmable chip-select signals ($\overline{\text{FB\_CS}}5$ – $\overline{\text{FB\_CS}}0$)
- 8-bit, 16-bit, and 32-bit transfers
- Programmable burst and burst-inhibited transfers selectable for each chip-select and transfer direction
- Programmable address-setup time with reference to the assertion of a chip-select

- Programmable address-hold time with reference to the deassertion of a chip-select and transfer direction
- Extended address latch enable option to assist with glueless connections to synchronous and asynchronous memory devices

2.1.17 Watch dog

The Watchdog Timer (WDOG) keeps a watch on the system functioning and resets it in case of its failure.

The WDOG has the following features:

- Clock source input independent from CPU/bus clock. Choice from LPO, SIRC, external system clock or bus clock.
- Unlock sequence for allowing updates to write-once WDOG control/configuration bits.
- All WDOG control/configuration bits are writable once only within 128 bus clock cycles of being unlocked.
- Programmable time-out period specified in terms of number of WDOG clock cycles.
- Ability to test WDOG timer and reset with a flag indicating watchdog test.
- Windowed refresh option.
- Robust refresh mechanism.
- Count of WDOG resets as they occur.
- Configurable interrupt on time-out to provide debug breadcrumbs. This is followed by a reset after 128 bus clock cycles.

2.1.18 EWM

The External Watchdog Monitor (EWM) is a redundant watchdog system which is used to monitor external circuits, as well as the MCU software flow. This provides a back-up mechanism to the internal watchdog that resets the MCU's CPU and peripherals.

The EWM has the following features:

2.1.19 XRDC

The Extended Resource Domain Controller (XRDC) provides an integrated, scalable architectural framework for access control, system memory protection and peripheral isolation.

The XRDC has the following features:

2.1.20 MU

The Messaging Unit module enables two processors within the SoC to communicate and coordinate by passing messages (e.g. data, status and control) through the MU interface. The MU also provides the ability for one processor to signal the other processor using interrupts.

The MU has the following features:

2.1.21 SEMA42

The SEMA42 is a memory-mapped module that provides robust hardware support needed in multi-core systems for implementing semaphores and provides a simple mechanism to achieve "lock and unlock" operations via a single write access. The hardware semaphore module provides hardware-enforced gates as well as other useful system functions related to the gating mechanisms.

The SEMA42 has the following features:

2.1.22 TRGMUX

The trigger multiplexer (TRGMUX) module allows software to configure the trigger inputs for various peripherals.

The TRGMUX module allows software to select the trigger source for peripherals. Each peripheral has its own dedicated TRGMUX register.

2.2 Peripheral features

The following sections describe the features of each peripherals of the chip.

2.2.1 MSMC

The Multi-System Mode Controller (MSMC) is responsible for sequencing the MCU into and out of all stop and run power modes.

Specifically, it monitors events to trigger transitions between power modes while controlling the power, clocks, and memories of the MCU to achieve the power consumption and functionality of that mode. Additionally, the MSMC will arbitrate between multiple cores in the MCU to provide each with the most optimal power mode without negatively impacting the functionality of other cores.

2.2.2 CRC

This device contains one cyclic redundancy check (CRC) module which can generate 16/32-bit CRC code for error detection.

The CRC module provides a programmable polynomial and other parameters required to implement a 16-bit or 32-bit CRC standard.

The 16/32-bit code is calculated for 32 bits of data at a time.

The CRC module has the following features:

2.2.3 LPDAC

The 12-bit low power digital-to-analog converter (LPDAC) is a low-power, general-purpose DAC. The output of the DAC can be placed on an external pin or set as one of the inputs to the analog comparator or ADC.

DAC module has the following features:

2.2.4 eDMA and DMAMUX

The eDMA controller module enables fast transfers of data, which provides an efficient way to move blocks of data with minimal processor interaction. The eDMA1 controller in this device implements eight channels which can be routed from up to 32 DMA request sources through DMAMUX1 module for CM0+ core. The eDMA0 module implements 16 channels which can be routed from up to 64 DMA request sources through DMAMUX0 module for CM4 core. Some of the peripheral request sources

have asynchronous eDMA capability which can be used to wake MCU from Stop mode. The peripherals which have such capability include FlexIO, LPUART0, LPUART1, LPUART2, LPUART3, LPSPI0, LPSPI1, LPSPI2, LPSPI3, LPI2C0, LPI2C1, LPI2C2, LPI2C3, LPCMP0, LPCMP1, TPM0, TPM1, TPM2, TPM3, LPTMR0, LPTMR1, LPTMR2, LLWU0, LLWU1, I2S, PORTA-PORTE, ADC0, and LPDAC0. The DMA0 channel 0 to 3 can be periodically triggered by LPIT0 while DMA1 channel 0 to 3 by LPIT1 via DMA MUX.

eDMA module has the following features:

DMAMUX module has the following features:

- Up to 64 peripheral slots can be routed to 16 channels for DMAMUX0 and up to 32 peripheral slots can be routed to 8 channels for DMAMUX1.
- 16 independently selectable DMA channel routers for DMAMUX0 and 8 for DMAMUX1.
- Each channel router can be assigned to one of the possible peripheral DMA slots.
  • On every memory map configuration change for a any channel, this module signals to the DMA Controller to reset the internal state machine for that channel and it can accept a new request based on the new configuration.

2.2.5 EMV SIM

The EMV SIM (Euro/Mastercard/Visa Serial Interface Module) is designed to facilitate communication to Smart Cards compatible to the EMV ver4.3 standard (Book 1) and Smart Cards compatible with ISO/IEC 7816-3 Standard.

EMV-SIM module has the following features:

2.2.6 FlexIO

The FlexIO is a highly configurable module providing a wide range of protocols including, but not limited to LPUART, I2C, SPI, I2S, Camera IF, LCD RGB, PWM/ Waveform generation. The module supports programmable baud rates independent of bus clock frequency, with automatic start/stop bit generation. It also supports to work in VLPR, VLPW, Stop, and VLPS modes when clock source remains enabled.

The FlexIO module has the following features:

2.2.7 ADC

This device contains one low power ADC module. This LPADC module supports hardware triggers from TRGMUX. It supports wakeup of MCU in low power mode when using internal clock source or external crystal clock.

ADC module has the following features:

2.2.8 LPCMP

The device contains two low power comparator modules which provide circuits for comparing two analog input voltages. Each comprises a comparator (CMP), a DAC and an analog mux (ANMUX).

The CMP circuit operates across the full range of the supply voltage. The DAC is a 64-tap resistor ladder network that provides a selectable voltage reference for applications requiring a voltage reference. The Analog MUX (ANMUX) provides a circuit for selecting an analog input signal from eight channels.

The CMP has the following features:

2.2.9 LPI2C

This device contains four LPI2C modules, which supports an efficient interface to an I2C bus as a master and/or a slave. The LPI2C can continue operating in stop modes provided an appropriate clock is available and is designed for low CPU overhead with DMA offloading of FIFO register accesses. The LPI2C implements logic support for standard-mode, fast-mode, fast-mode plus and ultra-fast modes of operation. The LPI2C module also complies with the System Management Bus (SMBus) Specification, version 2.

The LPI2C modules have the following features:

2.2.10 LPIT

This device contains two LPIT modules which are multi-channel timer modules generating independent pre-trigger and trigger outputs. These timer channels can operate individually or can be chained together. The LPIT can operate in low power modes if configured to do so. The pre-trigger and trigger outputs can be used to trigger other modules on the device.

Each timer channel can be configured to run independently and made to work in either compare or capture modes.

The timer channels operate on an asynchronous clock, which is independent from the register read/write access clock. Clock synchronization between the clock domains ensures normal operations.

2.2.11 LPSPI

This device contains four low power Serial Peripheral Interface (SPI) module that supports an efficient interface to an SPI bus as a master and/or a slave. The LPSPI can continue operating in stop modes provided an appropriate clock is available and is designed for low CPU overhead with DMA offloading of FIFO register accesses.

The LPSPI modules have the following features:

2.2.12 LPTMR

This device contains three low-power timer (LPTMR) which can be configured to operate as a time counter with optional prescaler, or as a pulse counter with optional glitch filter, across all power modes, including the low-leakage modes. It can also continue operating through most system reset events, allowing it to be used as a time of day counter.

The LPTMR module has the following features:

2.2.13 LPUART

This product contains four Low-Power UART modules, their clock sources are selectable from LPFLL, SIRC, FIRC and SOSC, and can work in Stop and VLPS modes. They also support 4x to 32x data oversampling rate to meet different applications.

The LPUART module has the following features:

2.2.14 RTC

The RTC is an always powered-on block that remains active in all low power modes. The time counter within the RTC is clocked by a 32.768 kHz clock sourced from an external crystal using the oscillator or clock directly from EXTAL32 pin.

RTC is reset on power-on reset, and a software reset bit in RTC can also initialize all RTC registers. During chip power-down, RTC is powered from the backup power supply (VBAT), electrically isolated from the rest of the chip, continues to increment the time counter (if enabled) and retain the state of the RTC registers. The RTC registers are not accessible.

The RTC module has the following features:

2.2.15 I2S

This device contains one Inter-IC Sound (I2S) module which provides a synchronous audio interface (SAI) that supports fullduplex serial interfaces with frame synchronization such as I2S, AC97, TDM, and codec/DSP interfaces.

I2S module has the following features:

2.2.16 uSDHC

The Ultra Secured Digital Host Controller (uSDHC) provides the interface between the host system and the SD/SDIO/MMC cards.

The uSDHC module has the following features:

- Conforms to the SD Host Controller Standard Specification version 2.0
- Compatible with the MMC System Specification version 4.2/4.3/4.4/4.41
- Compatible with the SD Memory Card Specification version 2.0 and supports the Extended Capacity SD Memory Card
- Compatible with the SDIO Card Specification version 2.0
- Designed to work with SD Memory, miniSD Memory, SDIO, miniSDIO, SD Combo, MMC, MMC plus, and MMC RS cards
- Card bus clock frequency up to 48 MHz
- Supports 1-bit / 4-bit SD and SDIO modes, 1-bit / 4-bit / 8-bit MMC modes
- Supports single block/multi-block read and write
- Supports block sizes of 1 ~ 4096 bytes
- Supports the write protection switch for write operations
- Supports both synchronous and asynchronous abort

- Supports pause during the data transfer at block gap
- Supports SDIO Read Wait and Suspend Resume operations
- Supports Auto CMD12 for multi-block transfer
- Host can initiate non-data transfer command while data transfer is in progress
- Allows cards to interrupt the host in 1-bit and 4-bit SDIO modes, also supports interrupt period
- Embodies a fully configurable 128x32-bit FIFO for read/write data
- Supports internal DMA capabilities
- Support voltage selection by configuring vendor specific register bit
- Supports Advanced DMA to perform linked memory access

2.2.17 TPM

This device contains four low power TPM modules (TPM) which support input capture, output compare, and the generation of PWM signals to control electric motor and power management applications. TPM0 and TPM2 have six channels while TPM1 and TPM3 have two channels.

The TPM modules have the following features:

2.2.18 TRNG

The Standalone True Random Number Generator (SA-TRNG) is a hardware accelerator module that generates a 128-bit entropy as needed by an entropy-consuming module or by other post-processing functions.

2.2.19 USB

This device contains one USB module which implements a USB2.0 full-speed compliant peripheral and interfaces to the on-chip USBFS transceiver. It implements keep-alive feature to avoid re-enumerating when exiting from low power modes and enables FIRC48M to allow crystal-less USB operation.

The USBFS has the following features:

- USB 1.1 and 2.0 compatible FS device
- 16 bidirectional endpoints
- DMA or FIFO data stream interfaces
- Low-power consumption

- IRC48M with clock-recovery is supported to eliminate the 48 MHz crystal. It is used for USB device-only implementation.
- Keep-alive feature is supported to power down system bus and CPU. USB can respond to IN with NAK and wake up for SETUP/OUT.

2.2.20 VREF

The VREF can be used in applications to provide a reference voltage to external devices, or used internally in the device as a reference to analog peripherals (such as the ADC, LPDAC, or LPCMP). The Voltage Reference (VREF) can supply an accurate voltage output that can be trimmed in 0.5 mV steps (for 1.2 V output) or 1.5 mV steps (for 2.1 V output). The voltage reference has 3 operating modes that provide different levels of supply rejection and power consumption.

The VREF supports the following features:

A 100 nF capacitor must always be connected between VERF output (VREFO) pin and VSSA if the VREF is used. This capacitor must be as close to VREFO pin as possible.

2.2.21 TSTMR

The Time Stamp Timer (TSTMR) is a 56-bit clock cycle counter, reset by system reset.

The TSTMR has the following features:

2.2.22 CAU3

The Version 3 Cryptographic Acceleration Unit (CAU3) is a bus mastering IP module that provides hardware acceleration of a variety of cryptographic symmetric key and secure hash algorithms including DES, 3DES, AES-{128,192,256}, SHA-{1,256,512} as well as acceleration of basic public key cryptography including Elliptical Curve Cryptography (ECC). The execution of these algorithms is controlled by optimized firmware developed by NXP that executes on the CAU3 module.

The CAU3 has the following features:

- Symmetric key functions: DES, 3DES, AES-{128,192,256}
- Secure hash functions: SHA-1, SHA-256
- Supoort SHA-512 secure hash acceleration
- AES-CBC, AES-CCM, AES-GCM

- RSA and ECC acceleration
- Programmable task completion signaling: interrupt, event completion, DMA request
- Significantly improved performance and power efficiency
- Common, portable CAU3 library written in C
- ARM embedded TLS library reference design

2.2.23 Radio

This device supports the 3rd generation 2.4 GHz Multi-Protocol Radio. The Radio is comprised of a Constant-Envelope Transmitter and a Quadrature Zero-IF Receiver and supports the modes described below in the 2.4 GHz ISM band.

Operating frequencies:

- 2.4 GHz ISM band (2400-2483.5 MHz)
- MBAN 2360-2400 MHz

Supported standards:

- Bluetooth v5.0 Low Energy compliant supporting up to 8 simultaneous connections in hardware (master-slave, master-master, slave-slave)
- Generic FSK modulation supporting up to 2 Mb/s data rate
- IEEE Standard 802.15.4-2011 compliant O-QPSK modulation and security features
- Thread Networking Stack
- Bluetooth Low Energy(BLE) Application Profiles

Receiver performance:

- Receive sensitivity of -96 dBm for BLE
- Receive sensitivity of -100 dBm typical for IEEE Standard 802.15.4
- Receive sensitivity of up to -100 dBm for a 250 kbps GFSK mode with a modulation index of 0.5. Receive sensitivity in generic FSK modes depends on mode selection and data rate.

Other features:

- Programmable transmit output power from -30 dBm to 3.5 dBm
- Integrated on-chip balun
- Single ended bidirectional RF port shared by transmit and receive
- Low external component count
- Supports transceiver range extension using external PA and/or LNA

- 26 and 32 MHz supported for BLE and FSK modes
- 32 MHz supported for IEEE Standard 802.15.4
- Bluetooth Low Energy ver. 5.0 Link Layer hardware with 8 independent hardware connection engines
- Hardware acceleration for IEEE Standard 802.15.4 packet processing/link layer
- Hardware acceleration for Generic FSK packet processing
- Supports dual PAN for IEEE Standard 802.15.4 with hardware-assisted address matching acceleration
- Generic FSK modulation at 250, 500, 1000 and 2000 kb/s
- Supports antenna diversity option for IEEE Std. 802.15.4

2.2.24 Transceiver

- Direct Conversion Receiver
- Constant Envelope Transmitter
- 2.36 GHz to 2.483 GHz PLL Range
- Low Transmit and Receive Current Consumption
- Low BOM

2.2.24.1 Key Specifications

This device meets or exceeds all Bluetooth Low Energy v5.0 and IEEE 802.15.4 performance specifications applicable to 2.4 GHz ISM and MBAN (Medical Band Area Network) bands. Key specifications are:

Frequency Band:

- ISM Band: 2400 to 2483.5MHz
- MBAN Band: 2360 to 2400MHz

Bluetooth Low Energy v5.0 modulation scheme:

- Symbol rate: 1000 kbps
- Modulation: GFSK
- Receiver sensitivity: -96 dBm, typical
- Programmable transmitter output power: -30 dBm to 3.5 dBm

IEEE Standard 802.15.4 2.4 GHz modulation scheme:

- Chip rate: 2000 kbps
- Data rate: 250 kbps

- Symbol rate: 62.5 kbps
- Modulation: OQPSK
- Receiver sensitivity: -100 dBm, typical (@1% PER for 20 byte payload packet)
- Single ended bidirectional RF input/output port with integrated transmit/receive switch
- Programmable transmitter output power: -30 dBm to 3.5 dBm

Generic FSK modulation scheme:

- Symbol rate: 250, 500, 1000 and 2000 kbps
- Modulation(s): GFSK (modulation index = 0.32, 0.5, 0.7 and 1.0, BT =0.5, 0.3 and 0.7), MSK
- Receiver Sensitivity: Mode and data rate dependant. -100 dBm typical for GFSK (r=250 kbps, BT = 0.5, h = 0.5)

2.2.24.2 Channel map frequency plans

2.2.24.2.1 Channel Plan for Bluetooth Low Energy

This section describes the frequency plan / channels associated with 2.4GHz ISM and MBAN bands for Bluetooth Low Energy.

2.4GHz ISM Channel numbering:

- Fc=2402 + k * 2 MHz, k=0,.....,39.

MBAN Channel numbering:

- Fc=2363 + 5*k in MHz, for k=0,.....,6
- Fc=2367 + 5*(k-7) in MHz, for k=7,8.....,13)

where k is the channel number.

Table 14. 2.4 GHz ISM and MBAN frequency plan and channel designations

2.4 GHz ISM[1]		MBAN[2]		2.4GHz ISM + MBAN	
Channel	Freq (MHz)	Channel	Freq (MHz)	Channel	Freq (MHz)
0	2402	0	2360	28	2390
1	2404	1	2361	29	2391
2	2406	2	2362	30	2392
3	2408	3	2363	31	2393

Table continues on the next page...

Table 14. 2.4 GHz ISM and MBAN frequency plan and channel designations (continued)

2.4 GHz ISM[1]		MBAN[2]		2.4GHz ISM + MBAN	
Channel	Freq (MHz)	Channel	Freq (MHz)	Channel	Freq (MHz)
4	2410	4	2364	32	2394
5	2412	5	2365	33	2395
6	2414	6	2366	34	2396
7	2416	7	2367	35	2397
8	2418	8	2368	36	2398
9	2420	9	2369	0	2402
10	2422	10	2370	1	2404
11	2424	11	2371	2	2406
12	2426	12	2372	3	2408
13	2428	13	2373	4	2410
14	2430	14	2374	5	2412
15	2432	15	2375	6	2414
16	2434	16	2376	7	2416
17	2436	17	2377	8	2418
18	2438	18	2378	9	2420
19	2440	19	2379	10	2422
20	2442	20	2380	11	2424
21	2444	21	2381	12	2426
22	2446	22	2382	13	2428
23	2448	23	2383	14	2430
24	2450	24	2384	15	2432
25	2452	25	2385	16	2434
26	2454	26	2386	17	2436
27	2456	27	2387	18	2438
28	2458	28	2388	19	2440
29	2460	29	2389	20	2442
30	2462	30	2390	21	2444
31	2464	31	2391	22	2446
32	2466	32	2392	23	2448
33	2468	33	2393	24	2450
34	2470	34	2394	25	2452
35	2472	35	2395	26	2454
36	2474	36	2396	27	2456
37	2476	37	2397	37	2476
38	2478	38	2398	38	2478
39	2480	39	2399	39	2480

1. ISM frequency of operation spans from 2400.0 MHz to 2483.5 MHz

2. Per FCC guideline rules, IEEE (R) 802.15.1 and Bluetooth Low Energy single mode operation is allowed in these channels.

2.2.24.2.2 Channel Plan for IEEE 802.15.4 in 2.4GHz ISM and MBAN frequency bands

This section describes the frequency plan / channels associated with 2.4GHz ISM and MBAN bands for IEEE 802.15.4.

2.4GHz ISM Channel numbering:

- Fc=2405 + 5*(k-11) MHz, k=11, 12, ..,26.

MBAN Channel numbering:

- Fc=2363.0 + 5*k in MHz, for k=0,.....,6
- Fc=2367.0 + 5*(k-7) in MHz, for k=7,.....,14

where k is the channel number.

Table 15. 2.4 GHz ISM and MBAN frequency plan and channel designations

2.4 GHz ISM		MBAN[1]	
Channel #	Frequency (MHz)	Channel #	Frequency (MHz)
11	2405	0	2363
12	2410	1	2368
13	2415	2	2373
14	2420	3	2378
15	2425	4	2383
16	2430	5	2388
17	2435	6	2393
18	2440	7	2367
19	2445	8	2372
20	2450	9	2377
21	2455	10	2382
22	2460	11	2387
23	2465	12	2392
24	2470	13	2397
25	2475	14	2395
26	2480		

1. Usable channel spacing to assit in co-existence.

2.2.24.2.3 Other Channel Plans

The RF synthesizer can be configured to use any channel frequency between 2.36 and 2.487 GHz.

2.2.24.3 Transceiver Functions

Receive

The receiver architecture is Zero IF (ZIF) where the received signal after passing through RF front end is down-converted to a baseband signal. The signal is filtered and amplified before it is fed to analog-to-digital converter. The digital signal is then decimated to a baseband clock frequency before it is digitally processed, demodulated and passed on to packet processing/link-layer processing.

Transmit

The transmitter transmits O-QPSK or GFSK/FSK modulation having power and channel selection adjustment per user application. After the channel of operation is determined, coarse and fine tuning is executed within the Frac-N PLL to engage signal lock. After signal lock is established, the modulated buffered signal is then routed to a multi-stage amplifier for transmission. The differential signals at the output of the PA (RF_P, RF_N) are converted to a single ended(SE) output signal by an on-chip balun.

2.3 Memory map

This device contains various memories and memory-mapped peripherals which are located in a 4 GB memory space. The following figure shows the system memory and peripheral locations

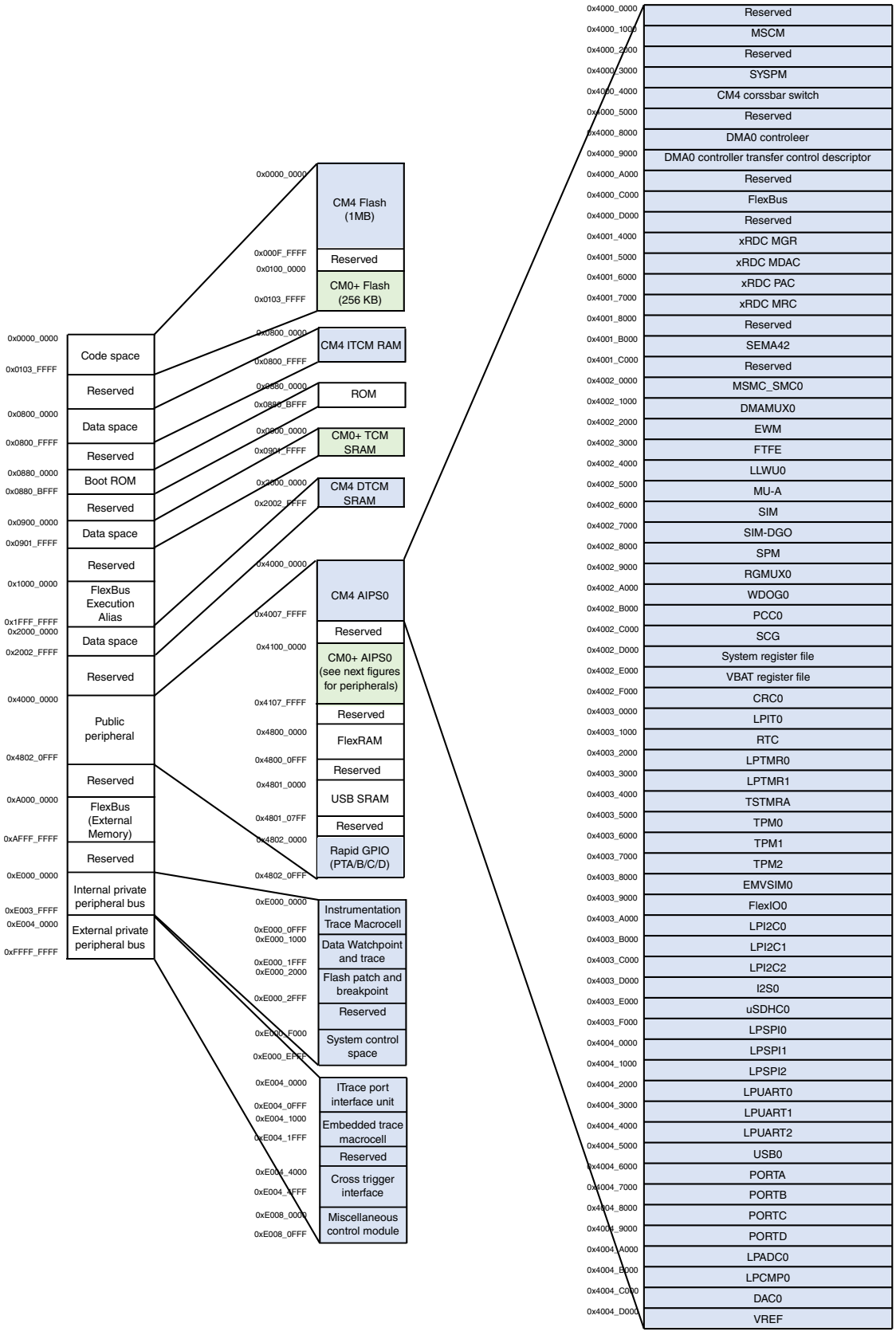


Figure 5. Memory map (CM4)

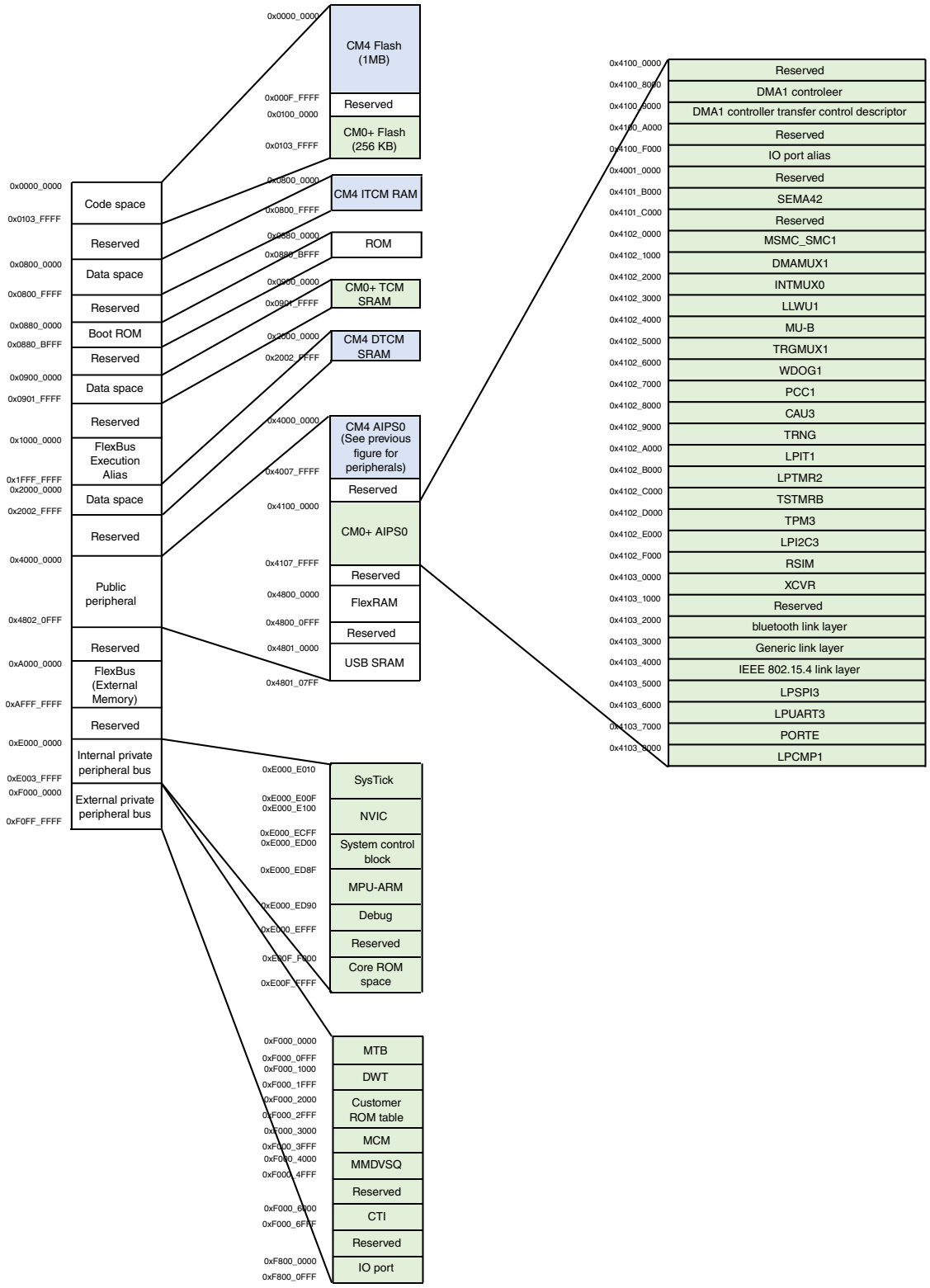


Figure 6. Memory map (CM0+)

3 Pinouts

3.1 RV32M1 subfamily Pinout

Table 16. RV32M1 Pinout

176 VFBGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
C1	PTB3	LPADC0_SE0	LPADC0_SE0	PTB3/ RF0_EXT_OSC_EN	LPSPI0_PCS3	LPUART1_TX	I2S0_TX_FS	FB_AD10	TPM0_CH1	—
C2	PTB4/ LLWU_P6	LPADC0_SE1	LPADC0_SE1	PTB4/ LLWU_P6/ RF0_RF_OFF/ RF0_DFT_RESET	LPSPI0_SCK	LPUART1_CTS	I2S0_TX_BCLK	FB_AD9	TPM0_CH2	—
D2	PTB5	DISABLED	—	PTB5/ RF0_ACTIVE	LPSPI0_SOUT	LPUART1_RTS	I2S0_MCLK	FB_AD8	TPM0_CH3	—
E1	PTB6/ LLWU_P7	DISABLED	—	PTB6/ LLWU_P7	LPSPI0_PCS2	LPI2C1_SDA	I2S0_RX_BCLK	FB_AD7	TPM0_CH4	RF0_BSM_FRAME
E2	PTB7/ LLWU_P8	LPADC0_SE2	LPADC0_SE2	PTB7/ LLWU_P8	LPSPI0_SIN	LPI2C1_SDAS	I2S0_RX_FS	FB_AD6	TPM0_CH5	RF0_BSM_DATA
F5	PTB8/ LLWU_P9	DISABLED	—	PTB8/ LLWU_P9/ RF0_EARLY_WARNING	LPSPI0_PCS0	LPI2C1_SCLS	I2S0_RXD0	FB_AD5	—	LPTMR0_ALT1
F4	PTB9	LPADC0_SE3	LPADC0_SE3	PTB9/ SPM_LPREQ	LPSPI0_PCS1	LPI2C1_SCL	I2S0_RXD1	FB_RW_b	—	FXIO0_D0
D5	VSS	VSS	VSS	—	—	—	—	—	—	—
C9	VDDIO1	VDDIO1	VDDIO1	—	—	—	—	—	—	—
G6	PTB11	DISABLED	—	PTB11	LPUART2_RX	LPI2C1_SDAS	LPI2C0_SDA	FB_AD27	—	FXIO0_D1
G4	PTB12	DISABLED	—	PTB12	LPUART2_TX	LPI2C1_SCLS	LPI2C0_SCL	FB_AD26	TPM3_CLKIN	FXIO0_D2
G3	PTB13	DISABLED	—	PTB13	LPUART2_CTS	LPI2C1_SDA	LPI2C0_SDAS	FB_AD25	TPM3_CH0	FXIO0_D3

Table continues on the next page...

Table 16. RV32M1 Pinout (continued)

176 VFBGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
G2	PTB14	DISABLED	—	PTB14	LPUART2_RTS	LPI2C1_SCL	LPI2C0_SCLS	FB_AD24	TPM3_CH1	FXIO0_D4
G1	PTB15	DISABLED	—	PTB15	—	LPI2C1_HREQ	LPI2C3_SCL	FB_CS5_b/ FB_TSIZ1/ FB_BE23_16_b	TPM0_CLKIN	FXIO0_D5
H5	PTB16/ LLWU_P10	DISABLED	—	PTB16/ LLWU_P10	—	LPUART3_CTS	LPI2C3_SDA	FB_CS4_b/ FB_TSIZ0/ FB_BE31_24_b	—	FXIO0_D6
K5	PTB17	DISABLED	—	PTB17	—	LPUART3_RTS	LPI2C3_SCLS	FB_TBST_b/ FB_CS2_b/ FB_BE15_8_b	—	FXIO0_D7
H2	PTB18	DISABLED	—	PTB18	LPSPI1_PCS1	LPUART2_RX	LPI2C3_SDAS	FB_CS3_b/ FB_BE7_0_b	FB_TA_b	FXIO0_D8
K4	PTB19	DISABLED	—	PTB19	LPSPI1_PCS3	LPUART2_TX	—	FB_ALE/ FB_CS1_b/ FB_TS_b	TPM1_CLKIN	FXIO0_D9
J1	PTB20/ LLWU_P11	DISABLED	—	PTB20/ LLWU_P11	LPSPI1_SCK	LPUART2_CTS	—	FB_CS0_b	TPM1_CH0	FXIO0_D10
J2	PTB21	DISABLED	—	PTB21	LPSPI1_SOUT	LPUART2_RTS	LPI2C2_HREQ	FB_AD4	TPM1_CH1	FXIO0_D11
L1	PTB22/ LLWU_P12	DISABLED	—	PTB22/ LLWU_P12	LPSPI1_PCS2	LPUART0_CTS	LPI2C2_SDA	FB_AD3	TPM2_CLKIN	FXIO0_D12
J4	VSS	VSS	VSS	—	—	—	—	—	—	—
J3	VDDIO1	VDDIO1	VDDIO1	—	—	—	—	—	—	—
L2	PTB24	DISABLED	—	PTB24	LPSPI1_SIN	LPUART0_RTS	LPI2C2_SCL	FB_AD2	EWM_IN	FXIO0_D13
L6	PTB25/ LLWU_P13	DISABLED	—	PTB25/ LLWU_P13	LPSPI1_PCS0	LPUART0_RX	LPI2C2_SDAS	FB_AD1	EWM_OUT_b	FXIO0_D14
L4	PTB26	DISABLED	—	PTB26	USB0_SOF_OUT	LPUART0_TX	LPI2C2_SCLS	FB_AD0	LPCMP0_OUT	RF0_BSM_CLK

Table continues on the next page...

Table 16. RV32M1 Pinout (continued)

176 VFBGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
M4	PTB28/ LLWU_P14	DISABLED	—	PTB28/ LLWU_P14	—	LPUART3_RX	I2S0_TXD0	FB_A16	—	FXIO0_D15
L3	PTB29	DISABLED	—	PTB29	—	LPUART3_TX	I2S0_TX_FS	FB_A17	—	FXIO0_D16
M5	PTB30	DISABLED	—	PTB30	—	—	I2S0_TX_BCLK	FB_A18	—	—
M7	PTB31	DISABLED	—	PTB31	—	—	I2S0_RXD0	FB_A19	—	—
N1	PTC0	DISABLED	—	PTC0	—	—	I2S0_RX_FS	FB_A20	—	—
M2	PTC1	DISABLED	—	PTC1	—	—	I2S0_RX_BCLK	FB_A21	—	—
N3	VSS	VSS	VSS	—	—	—	—	—	—	—
J10	VDDIO1	VDDIO1	VDDIO1	—	—	—	—	—	—	—
N2	PTC7/ LLWU_P15	LPCMP0_IN0	LPCMP0_IN0	PTC7/ LLWU_P15	LPSPI0_PCS3	LPUART0_RX	LPI2C1_HREQ	—	TPM0_CH0	LPTMR1_ALT1
P3	PTC8	LPCMP0_IN1	LPCMP0_IN1	PTC8	LPSPI0_SCK	LPUART0_TX	LPI2C0_HREQ	—	TPM0_CH1	—
R1	PTC9/ LLWU_P16	LPADC0_SE4/ LPCMP0_IN2	LPADC0_SE4/ LPCMP0_IN2	PTC9/ LLWU_P16	LPSPI0_SOUT	LPUART0_CTS	LPI2C0_SDA	—	TPM0_CH2	LPTMR0_ALT2
R2	PTC10	LPADC0_SE5	LPADC0_SE5	PTC10	LPSPI0_PCS2	LPUART0_RTS	LPI2C0_SCL	—	TPM0_CH3	—
T1	PTC11/ LLWU_P17	LPADC0_SE6	LPADC0_SE6	PTC11/ LLWU_P17	LPSPI0_SIN	LPI2C1_SDA	LPI2C0_SDAS	—	TPM0_CH4	EWM_IN
R3	PTC12/ LLWU_P18	LPADC0_SE7	LPADC0_SE7	PTC12/ LLWU_P18	LPSPI0_PCS0	LPI2C1_SCL	LPI2C0_SCLS	—	TPM0_CH5	EWM_OUT_b
U1	VDD_DCDC	VDD_DCDC	VDD_DCDC	—	—	—	—	—	—	—
U2	LP	LP	LP	—	—	—	—	—	—	—
U3	GND	GND	GND	—	—	—	—	—	—	—
T4	LN	LN	LN	—	—	—	—	—	—	—
T3	VOUT_RF	VOUT_RF	VOUT_RF	—	—	—	—	—	—	—
T5	VOUT_CORE	VOUT_CORE	VOUT_CORE	—	—	—	—	—	—	—
R9	VDDIO1	VDDIO1	VDDIO1	—	—	—	—	—	—	—
P9	VSS	VSS	VSS	—	—	—	—	—	—	—

Table continues on the next page...

Table 16. RV32M1 Pinout (continued)

176 VFBGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
N15	VDD_CORE	VDD_CORE	VDD_CORE	—	—	—	—	—	—	—
P6	PTC27	DISABLED	—	PTC27	—	—	—	—	TPM0_CH4	—
U5	PTC28	DISABLED	—	PTC28	—	LPSPI0_PCS1	—	—	TPM0_CH3	FXIO0_D17
N6	PTC29	DISABLED	—	PTC29	LPUART1_RX	LPSPI0_PCS3	—	—	TPM0_CH2	FXIO0_D18
R7	PTC30	DISABLED	—	PTC30	LPUART1_TX	LPSPI0_SCK	—	—	TPM0_CH1	FXIO0_D19
R5	VDDIO1	VDDIO1	VDDIO1	—	—	—	—	—	—	—
R13	VSS	VSS	VSS	—	—	—	—	—	—	—
T7	PTD0	DISABLED	—	PTD0	LPUART1_CTS	LPSPI0_SOUT	—	—	TPM0_CH0	FXIO0_D20
P7	PTD1	DISABLED	—	PTD1	LPUART1_RTS	LPSPI0_PCS2	—	—	EWM_IN	FXIO0_D21
U7	PTD2	DISABLED	—	PTD2	SDHC0_D7	LPSPI0_SIN	—	—	EWM_OUT_b	FXIO0_D22
T8	PTD3	DISABLED	—	PTD3	SDHC0_D6	LPSPI0_PCS0	EMVSIM0_CLK	—	TPM2_CLKIN	FXIO0_D23
N8	PTD4	DISABLED	—	PTD4	SDHC0_D5	LPSPI2_PCS1	EMVSIM0_RST	—	—	FXIO0_D24
N10	PTD5	LPADC0_SE8	LPADC0_SE8	PTD5	SDHC0_D4	LPSPI2_PCS3	EMVSIM0_VCCEN	—	—	FXIO0_D25
U9	PTD6	LPADC0_SE9	LPADC0_SE9	PTD6	SDHC0_D1	LPSPI2_SCK	EMVSIM0_IO	TRACE_D3	TPM2_CH5	FXIO0_D26
P10	PTD7	LPADC0_SE10	LPADC0_SE10	PTD7	SDHC0_D0	LPSPI2_SOUT	EMVSIM0_PD	TRACE_D2	TPM2_CH4	FXIO0_D27
T9	PTD8/LLWU_P19	LPADC0_SE11	LPADC0_SE11	PTD8/LLWU_P19	SDHC0_DCLK	LPSPI2_PCS2	LPI2C1_SDAS	TRACE_D1	TPM2_CH3	FXIO0_D28
U11	PTD9	LPADC0_SE12	LPADC0_SE12	PTD9	SDHC0_CMD	LPSPI2_SIN	LPI2C1_SCLS	TRACE_D0	TPM2_CH2	FXIO0_D29
P11	PTD10/LLWU_P20	LPADC0_SE13	LPADC0_SE13	PTD10/LLWU_P20	SDHC0_D3	LPSPI2_PCS0	LPI2C1_SDA	TRACE_CLKOUT	TPM2_CH1	FXIO0_D30
R11	PTD11	LPADC0_SE14	LPADC0_SE14	PTD11	SDHC0_D2	USB0_SOF_OUT	LPI2C1_SCL	CLKOUT	TPM2_CH0	FXIO0_D31
P5	VDDIO1	VDDIO1	VDDIO1	—	—	—	—	—	—	—
P13	VSS	VSS	VSS	—	—	—	—	—	—	—
N4	USB0_VSS	USB0_VSS	USB0_VSS	—	—	—	—	—	—	—

Table continues on the next page...

Table 16. RV32M1 Pinout (continued)

176 VFBGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
T11	USB0_DP	USB0_DP	USB0_DP	—	—	—	—	—	—	—
T12	USB0_DM	USB0_DM	USB0_DM	—	—	—	—	—	—	—
T13	VOUT33	VOUT33	VOUT33	—	—	—	—	—	—	—
U13	VREGIN	VREGIN	VREGIN	—	—	—	—	—	—	—
U15	VDDA	VDDA	VDDA	—	—	—	—	—	—	—
U16	VREFH	VREFH	VREFH	—	—	—	—	—	—	—
T15	VREF_OUT	VREF_OUT/ LPADC0_SE15/ LPCMP0_IN5/ LPCMP1_IN5	VREF_OUT/ LPADC0_SE15/ LPCMP0_IN5/ LPCMP1_IN5	—	—	—	—	—	—	—
U17	VREFL	VREFL	VREFL	—	—	—	—	—	—	—
T16	VSSA	VSSA	VSSA	—	—	—	—	—	—	—
T17	DAC0_OUT	DAC0_OUT/ LPADC0_SE16/ LPCMP0_IN3/ LPCMP1_IN3	DAC0_OUT/ LPADC0_SE16/ LPCMP0_IN3/ LPCMP1_IN3	—	—	—	—	—	—	—
R14	PTE0	LPCMP1_IN4	LPCMP1_IN4	PTE0	—	—	—	—	EWM_IN	—
R16	PTE1/ LLWU_P21	LPADC0_SE18	LPADC0_SE18	PTE1/ LLWU_P21	SDHC0_D1	LPI2C0_SDAS	LPSPI3_PCS1	—	EWM_OUT_b	LPTMR1_ALT2
P12	PTE2	LPADC0_SE19	LPADC0_SE19	PTE2	SDHC0_D0	LPI2C0_SCLS	LPSPI3_PCS3	—	LPCMP1_OUT	—
N12	PTE3/ LLWU_P22	LPADC0_SE20/ LPCMP1_IN0	LPADC0_SE20/ LPCMP1_IN0	PTE3/ LLWU_P22	SDHC0_D7	LPI2C0_SDA	LPSPI3_SCK	—	TPM0_CLKIN	LPTMR0_ALT3
M11	PTE4	LPADC0_SE21/ LPCMP1_IN1	LPADC0_SE21/ LPCMP1_IN1	PTE4	SDHC0_D6	LPI2C0_SCL	LPSPI3_SOUT	CLKOUT	TPM1_CLKIN	RF0_DTM_RX
R17	PTE5	LPCMP1_IN2	LPCMP1_IN2	PTE5	SDHC0_DCLK	LPI2C0_HREQ	LPSPI3_PCS2	—	LPCMP1_OUT	RF0_DTM_TX
J8	VDD_CORE	VDD_CORE	VDD_CORE	—	—	—	—	—	—	—

Table continues on the next page...

Table 16. RV32M1 Pinout (continued)

176 VFBGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
K10	VSS	VSS	VSS	—	—	—	—	—	—	—
D13	VDDIO2	VDDIO2	VDDIO2	—	—	—	—	—	—	—
P16	PTE8/ LLWU_P 23	LPADC0 _SE22	LPADC0 _SE22	PTE8/ LLWU_P 23	SDHC0_ D5	LPUART 3_RX	LPSPI3_ SIN	—	TPM1_C H0	LPTMR2 _ALT1
N16	PTE9/ LLWU_P 24	LPADC0 _SE23	LPADC0 _SE23	PTE9/ LLWU_P 24	SDHC0_ CMD	LPUART 3_TX	LPSPI3_ PCS0	—	TPM1_C H1	FXIO0_D 0
M13	PTE10/ LLWU_P 25	DISABLE D	—	PTE10/ LLWU_P 25	SDHC0_ D4	LPUART 3_CTS	LPI2C3_ SDA	—	TPM3_C H0	LPTMR2 _ALT3
M14	PTE11	DISABLE D	—	PTE11	SDHC0_ D3	LPUART 3_RTS	LPI2C3_ SCL	—	TPM3_C H1	FXIO0_D 1
L12	PTE12/ LLWU_P 26	DISABLE D	—	PTE12/ LLWU_P 26	SDHC0_ D2	—	LPI2C3_ SDAS	—	TPM3_C LKIN	FXIO0_D 2
N17	PTE13	DISABLE D	—	PTE13	I2S0_TX _BCLK	—	LPI2C3_ SCLS	—	TPM3_C H0	FXIO0_D 3
L16	PTE14	DISABLE D	—	PTE14	I2S0_TX _FS	—	LPI2C3_ HREQ	—	TPM3_C H1	FXIO0_D 4
L17	PTE15	DISABLE D	—	PTE15	I2S0_TX D0	—	—	—	TPM3_C LKIN	FXIO0_D 5
L14	PTE16	DISABLE D	—	PTE16	I2S0_RX _BCLK	—	—	—	TPM2_C H0	FXIO0_D 6
L15	PTE17	DISABLE D	—	PTE17	I2S0_RX _FS	—	—	—	TPM2_C H1	FXIO0_D 7
K13	PTE18	DISABLE D	—	PTE18	I2S0_RX D0	—	—	—	TPM2_C H2	FXIO0_D 8
K16	PTE19	DISABLE D	—	PTE19	I2S0_MC LK	—	—	—	TPM2_C H3	FXIO0_D 9
J17	PTE21	DISABLE D	—	PTE21	I2S0_TX D1	USB0_S OF_OUT	—	—	TPM2_C H4	FXIO0_D 10
J16	PTE22	DISABLE D	—	PTE22	I2S0_RX D1	LPI2C3_ HREQ	—	—	TPM2_C H5	FXIO0_D 11
J14	VSS	VSS	VSS	—	—	—	—	—	—	—
J15	VDDIO2	VDDIO2	VDDIO2	—	—	—	—	—	—	—
H14	PTE27	DISABLE D	—	PTE27	LPUART 3_CTS	LPI2C3_ SDAS	—	—	—	FXIO0_D 28
G14	PTE28	DISABLE D	—	PTE28	LPUART 3_RTS	LPI2C3_ SCLS	—	—	—	FXIO0_D 29
G15	PTE29	DISABLE D	—	PTE29	LPUART 3_RX	LPI2C3_ SDA	—	—	—	FXIO0_D 30
G17	PTE30	DISABLE D	—	PTE30	LPUART 3_TX	LPI2C3_ SCL	—	—	TPM2_C LKIN	FXIO0_D 31

Table continues on the next page...

Table 16. RV32M1 Pinout (continued)

176 VFBGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
H13	TAMPER3	TAMPER3	TAMPER3	—	—	—	—	—	—	—
G12	TAMPER2	TAMPER2	TAMPER2	—	—	—	—	—	—	—
F13	TAMPER1/ RTC_CLKOUT	TAMPER1/ RTC_CLKOUT	TAMPER1/ RTC_CLKOUT	—	—	—	—	—	—	—
F14	TAMPER0/ RTC_WAKEUP_b	TAMPER0/ RTC_WAKEUP_b	TAMPER0/ RTC_WAKEUP_b	—	—	—	—	—	—	—
G16	VBAT	VBAT	VBAT	—	—	—	—	—	—	—
E17	XTAL32	XTAL32	XTAL32	—	—	—	—	—	—	—
E16	EXTAL32	EXTAL32	EXTAL32	—	—	—	—	—	—	—
E15	VSS	VSS	VSS	—	—	—	—	—	—	—
C17	VDD_RF	VDD_RF	VDD_RF	—	—	—	—	—	—	—
B17	VDD_RF	VDD_RF	VDD_RF	—	—	—	—	—	—	—
A16	GANT	GANT	GANT	—	—	—	—	—	—	—
A15	ANT	ANT	ANT	—	—	—	—	—	—	—
B13	VDD_RF	VDD_RF	VDD_RF	—	—	—	—	—	—	—
A11	XTAL_RF	XTAL_RF	XTAL_RF	—	—	—	—	—	—	—
B11	EXTAL_RF	EXTAL_RF	EXTAL_RF	—	—	—	—	—	—	—
C11	RF_CLKOUT	RF_CLKOUT	RF_CLKOUT	—	—	—	—	—	—	—
D12	RESET_b	RESET_b	RESET_b	—	—	—	—	—	—	—
B10	PTA0	NMI_b	—	PTA0	—	—	—	—	—	NMI_b
E12	PTA1/ LLWU_P0	JTAG_TCLK/ SWD_CLK	—	PTA1/ LLWU_P0/ RF_ANT_B	LPUART0_CTS	LPI2C0_SDAS	LPUART1_CTS	—	—	JTAG_TCLK/ SWD_CLK
F11	PTA2/ LLWU_P1	JTAG_TDI	—	PTA2/ LLWU_P1/ RF_ANT_A	LPUART0_RX	LPI2C0_SDA	LPUART1_RX	—	—	JTAG_TDI
D11	PTA3	JTAG_TDO/ SWD_SWO	—	PTA3/ RF0_TX_SWITCH	LPUART0_TX	LPI2C0_SCL	LPUART1_TX	—	TPM0_CLKIN	JTAG_TDO/ SWD_SWO

Table continues on the next page...

Table 16. RV32M1 Pinout (continued)

176 VFBGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
B9	PTA4	JTAG_TMS/SWD_DIO	—	PTA4/RF0_RX_SWITCH	LPUART0_RTS	LPI2C0_SCLS	LPUART1_RTS	—	LPCMP0_OUT	JTAG_TMS/SWD_DIO
H9	VDD_CORE	VDD_CORE	VDD_CORE	—	—	—	—	—	—	—
E14	VSS	VSS	VSS	—	—	—	—	—	—	—
K9	VDDIO1	VDDIO1	VDDIO1	—	—	—	—	—	—	—
E10	PTA9	RV_JTAG_TCLK	—	PTA9	LPI2C2_SDAS	LPSPI3_SCK	—	FB_A23	—	RV_JTAG_TCLK
A9	PTA10	RV_JTAG_TDI	—	PTA10	LPI2C2_SCLS	LPSPI3_SOUT	—	FB_A22	—	RV_JTAG_TDI
E8	PTA14	RV_JTAG_TDO	—	PTA14	LPI2C2_SDA	—	—	FB_AD23	LPCMP0_OUT	RV_JTAG_TDO
A7	PTA15	RV_JTAG_TMS	—	PTA15	LPI2C2_SCL	—	—	FB_AD22	—	RV_JTAG_TMS
A17	VSS	VSS	VSS	—	—	—	—	—	—	—
E4	VDDIO1	VDDIO1	VDDIO1	—	—	—	—	—	—	—
F7	PTA17	DISABLED	—	PTA17	LPI2C2_HREQ	LPSPI3_PCS1	EMVSIM0_CLK	FB_AD21	—	—
D8	PTA18	DISABLED	—	PTA18	LPSPI2_PCS1	LPSPI3_PCS3	EMVSIM0_RST	FB_AD20	—	—
D7	PTA19	DISABLED	—	PTA19	LPSPI2_PCS3	LPSPI3_SCK	EMVSIM0_VCCEN	FB_AD19	TPM2_CH5	—
C7	PTA20	DISABLED	—	PTA20	LPSPI2_SCK	LPSPI1_PCS1	EMVSIM0_IO	FB_AD18	TPM2_CH4	—
B7	PTA21	DISABLED	—	PTA21	LPSPI2_SOUT	—	EMVSIM0_PD	FB_AD17	TPM2_CH3	—
B6	PTA22/LLWU_P2	DISABLED	—	PTA22/LLWU_P2	LPSPI2_PCS2	—	LPI2C2_HREQ	FB_AD16	TPM2_CH2	—
E6	PTA23	DISABLED	—	PTA23	LPSPI2_SIN	LPSPI1_PCS3	LPI2C2_SDA	FB_AD15	TPM2_CH1	—
D6	PTA24	DISABLED	—	PTA24	LPSPI2_PCS0	LPSPI1_SCK	LPI2C2_SCL	FB_OE_b	TPM2_CH0	—
B5	PTA25	DISABLED	—	PTA25	LPUART1_RX	LPSPI3_SOUT	LPI2C2_SDAS	FB_AD31	—	—
A5	PTA26	DISABLED	—	PTA26	LPUART1_TX	LPSPI3_PCS2	LPI2C2_SCLS	FB_AD30	—	—
A3	PTA27	DISABLED	—	PTA27	LPUART1_CTS	LPSPI3_SIN	—	FB_AD29	—	—
A2	PTA28	DISABLED	—	PTA28	LPUART1_RTS	LPSPI3_PCS0	—	FB_AD28	—	—

Table continues on the next page...

Table 16. RV32M1 Pinout (continued)

176 VFBGA	Pin Name	DEFAULT	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7
A13	VSS	VSS	VSS	—	—	—	—	—	—	—
E3	VDDIO1	VDDIO1	VDDIO1	—	—	—	—	—	—	—
A1	PTA30/ LLWU_P3	DISABLED	—	PTA30/ LLWU_P3	LPUART2_CTS	LPSPI1_SOUT	—	FB_AD14	TPM1_CH0	LPTMR2_ALT2
C4	PTA31	DISABLED	—	PTA31	LPUART2_RTS	LPSPI1_PCS2	—	FB_AD13	TPM1_CH1	—
B3	PTB0	DISABLED	—	PTB0	LPUART2_TX	LPSPI1_SIN	USB0_SOF_OUT	CLKOUT	TPM1_CLKIN	—
C3	PTB1/ LLWU_P4	DISABLED	—	PTB1/ LLWU_P4	LPUART2_RX	LPSPI1_PCS0	I2S0_TXD1	FB_AD12	—	LPTMR1_ALT3
B1	PTB2/ LLWU_P5	DISABLED	—	PTB2/ LLWU_P5/ RF0_RFOSC_EN	LPSPI0_PCS1	LPUART1_RX	I2S0_TXD0	FB_AD11	TPM0_CH0	—
B14	VSS	VSS	VSS	—	—	—	—	—	—	—
B15	VSS	VSS	VSS	—	—	—	—	—	—	—
B16	VSS	VSS	VSS	—	—	—	—	—	—	—
C5	VSS	VSS	VSS	—	—	—	—	—	—	—
C13	VSS	VSS	VSS	—	—	—	—	—	—	—
C15	VSS	VSS	VSS	—	—	—	—	—	—	—
C16	VSS	VSS	VSS	—	—	—	—	—	—	—
D9	VSS	VSS	VSS	—	—	—	—	—	—	—
D15	VSS	VSS	VSS	—	—	—	—	—	—	—
F16	VSS	VSS	VSS	—	—	—	—	—	—	—
H8	VSS	VSS	VSS	—	—	—	—	—	—	—
H10	VSS	VSS	VSS	—	—	—	—	—	—	—
K8	VSS	VSS	VSS	—	—	—	—	—	—	—
N14	VDD_CORE	VDD_CORE	VDD_CORE	—	—	—	—	—	—	—
R15	VSSA	VSSA	VSSA	—	—	—	—	—	—	—
B2	PTA30/ LLWU_P3	DISABLED	—	PTA30/ LLWU_P3	LPUART2_CTS	LPSPI1_SOUT	—	FB_AD14	TPM1_CH0	LPTMR2_ALT2

3.2 Pin properties

The following table lists the pin properties.

176 VFBGA	Pin Name	Drive strength	Default status after POR	Pullup/ Pulldown enable after POR	Pullup/ pulldown selection after POR	Slew rate after POR	Passive pin filter after POR	Open drain enable at reset	Open drain enable control	Pin interrupt	Fast capability	Fast high drive
C1	PTB3	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
C2	PTB4/ LLWU_ P6	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
D2	PTB5	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
E1	PTB6/ LLWU_ P7	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
E2	PTB7/ LLWU_ P8	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
F5	PTB8/ LLWU_ P9	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
F4	PTB9	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
D5	VSS	—	—	—	—	—	—	—	—	—	—	—
C9	VDDIO1	—	—	—	—	—	—	—	—	—	—	—
G6	PTB11	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
G4	PTB12	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
G3	PTB13	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
G2	PTB14	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
G1	PTB15	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
H5	PTB16/ LLWU_ P10	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
K5	PTB17	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
H2	PTB18	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
K4	PTB19	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
J1	PTB20/ LLWU_ P11	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
J2	PTB21	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N

Table continues on the next page...

176 VFBGA	Pin Name	Drive strength	Default status after POR	Pullup/ Pulldown enable after POR	Pullup/ pulldown selection after POR	Slew rate after POR	Passive pin filter after POR	Open drain enable at reset	Open drain enable control	Pin interrupt	Fast capability	Fast high drive
L1	PTB22/ LLWU_ P12	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
J4[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
J3	VDDIO1	—	—	—	—	—	—	—	—	—	—	—
L2	PTB24	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
L6	PTB25/ LLWU_ P13	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
L4	PTB26	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
M4	PTB28/ LLWU_ P14	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
L3	PTB29	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
M5	PTB30	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
M7	PTB31	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
N1	PTC0	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
M2	PTC1	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
N3[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
J10	VDDIO1	—	—	—	—	—	—	—	—	—	—	—
N2	PTC7/ LLWU_ P15	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
P3	PTC8	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
R1	PTC9/ LLWU_ P16	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
R2	PTC10	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
T1	PTC11/ LLWU_ P17	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y

Table continues on the next page...

176 VFBGA	Pin Name	Drive strength	Default status after POR	Pullup/ Pulldown enable after POR	Pullup/ pulldown selection after POR	Slew rate after POR	Passive pin filter after POR	Open drain enable at reset	Open drain enable control	Pin interrupt	Fast capability	Fast high drive
R3	PTC12/ LLWU_ P18	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
U1	VDD_D CDC	—	—	—	—	—	—	—	—	—	—	—
U2	LP	—	—	—	—	—	—	—	—	—	—	—
U3	GND	—	—	—	—	—	—	—	—	—	—	—
T4	LN	—	—	—	—	—	—	—	—	—	—	—
T3	VOUT_ RF	—	—	—	—	—	—	—	—	—	—	—
T5	VOUT_ CORE	—	—	—	—	—	—	—	—	—	—	—
R9	VDDIO1	—	—	—	—	—	—	—	—	—	—	—
P9	VSS	—	—	—	—	—	—	—	—	—	—	—
N15	VDD_C ORE	—	—	—	—	—	—	—	—	—	—	—
—	PTC26	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
P6	PTC27	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
U5	PTC28	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
N6	PTC29	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
R7	PTC30	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
R5	VDDIO1	—	—	—	—	—	—	—	—	—	—	—
R13	VSS	—	—	—	—	—	—	—	—	—	—	—
T7	PTD0	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
P7	PTD1	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
U7	PTD2	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
T8	PTD3	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
N8	PTD4	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
N10	PTD5	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
U9	PTD6	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N

Table continues on the next page...

176 VFBGA	Pin Name	Drive strength	Default status after POR	Pullup/ Pulldown enable after POR	Pullup/ pulldown selection after POR	Slew rate after POR	Passive pin filter after POR	Open drain enable at reset	Open drain enable control	Pin interrupt	Fast capability	Fast high drive
P10	PTD7	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
T9	PTD8/ LLWU_ P19	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
U11	PTD9	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
P11	PTD10/ LLWU_ P20	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
R11	PTD11	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
P5	VDDIO1	—	—	—	—	—	—	—	—	—	—	—
P13[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
N4	USB0_ VSS	—	—	—	—	—	—	—	—	—	—	—
T11	USB0_ DP	—	—	—	—	—	—	—	—	—	—	—
T12	USB0_ DM	—	—	—	—	—	—	—	—	—	—	—
T13	VOUT33	—	—	—	—	—	—	—	—	—	—	—
U13	VREGIN	—	—	—	—	—	—	—	—	—	—	—
U15	VDDA	—	—	—	—	—	—	—	—	—	—	—
U16	VREFH	—	—	—	—	—	—	—	—	—	—	—
T15	VREF_ OUT	—	—	—	—	—	—	—	—	—	—	—
U17	VREFL	—	—	—	—	—	—	—	—	—	—	—
T16	VSSA	—	—	—	—	—	—	—	—	—	—	—
T17	DAC0_ OUT	—	—	—	—	—	—	—	—	—	—	—
R14	PTE0	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N

Table continues on the next page...

176 VFBGA	Pin Name	Drive strength	Default status after POR	Pullup/ Pulldown enable after POR	Pullup/ pulldown selection after POR	Slew rate after POR	Passive pin filter after POR	Open drain enable at reset	Open drain enable control	Pin interrupt	Fast capability	Fast high drive
R16	PTE1/ LLWU_ P21	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
P12	PTE2	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
N12	PTE3/ LLWU_ P22	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
M11	PTE4	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
R17	PTE5	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
J8	VDD_C ORE	—	—	—	—	—	—	—	—	—	—	—
K10[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
D13	VDDIO2	—	—	—	—	—	—	—	—	—	—	—
P16	PTE8/ LLWU_ P23	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
N16	PTE9/ LLWU_ P24	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
M13	PTE10/ LLWU_ P25	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
M14	PTE11	HD	Hi-Z	N	PD	FS	N	N	Y	Y	N	Y
L12	PTE12/ LLWU_ P26	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
N17	PTE13	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
L16	PTE14	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
L17	PTE15	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
L14	PTE16	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
L15	PTE17	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
K13	PTE18	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N

Table continues on the next page...

176 VFBGA	Pin Name	Drive strength	Default status after POR	Pullup/ Pulldown enable after POR	Pullup/ pulldown selection after POR	Slew rate after POR	Passive pin filter after POR	Open drain enable at reset	Open drain enable control	Pin interrupt	Fast capability	Fast high drive
K16	PTE19	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
J17	PTE21	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
J16	PTE22	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
J14[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
J15	VDDIO2	—	—	—	—	—	—	—	—	—	—	—
H14	PTE27	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
G14	PTE28	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
G15	PTE29	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
G17	PTE30	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
H13	TAMPER3	ND	Hi-Z	N	PU	FS	N	N	N	N	N	N
G12	TAMPER2	ND	Hi-Z	N	PU	FS	N	N	N	N	N	N
F13	TAMPER1/ RTC_CLKOUT	ND	Hi-Z	N	PU	FS	N	N	N	N	N	N
F14	TAMPER0/ RTC_WAKEUP_b	ND	Hi-Z	N	PU	FS	N	N	N	N	N	N
G16	VBAT	—	—	—	—	—	—	—	—	—	—	—
E17	XTAL32	—	—	—	—	—	—	—	—	—	—	—
E16	EXTAL32	—	—	—	—	—	—	—	—	—	—	—
E15	VSS	—	—	—	—	—	—	—	—	—	—	—
C17	VDD_RF	—	—	—	—	—	—	—	—	—	—	—
B17	VDD_RF	—	—	—	—	—	—	—	—	—	—	—
A16	GANT	—	—	—	—	—	—	—	—	—	—	—

Table continues on the next page...

176 VFBGA	Pin Name	Drive strength	Default status after POR	Pullup/ Pulldown enable after POR	Pullup/ pulldown selection after POR	Slew rate after POR	Passive pin filter after POR	Open drain enable at reset	Open drain enable control	Pin interrupt	Fast capability	Fast high drive
A15	ANT	—	—	—	—	—	—	—	—	—	—	—
B13	VDD_RF	—	—	—	—	—	—	—	—	—	—	—
A11	XTAL_RF	—	—	—	—	—	—	—	—	—	—	—
B11	EXTAL_RF	—	—	—	—	—	—	—	—	—	—	—
C11	RF_CLKOUT	—	—	—	—	—	—	—	—	—	—	—
D12	RESET_b	ND	H	N	PU	—	Y	—	—	—	—	—
B10	PTA0	ND	H	Y	PU	FS	N	N	Y	Y	N	N
E12	PTA1/ LLWU_P0	ND	L	Y	PD	FS	N	N	Y	Y	N	N
F11	PTA2/ LLWU_P1	ND	H	Y	PU	FS	N	N	Y	Y	N	N
D11	PTA3	ND	H	Y	PU	FS	N	N	Y	Y	N	N
B9	PTA4	ND	H	Y	PU	FS	N	N	Y	Y	N	N
H9	VDD_CORE	—	—	—	—	—	—	—	—	—	—	—
E14	VSS	—	—	—	—	—	—	—	—	—	—	—
K9	VDDIO1	—	—	—	—	—	—	—	—	—	—	—
E10	PTA9	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
A9	PTA10	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
E8	PTA14	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
A7	PTA15	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
A17[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
E4	VDDIO1	—	—	—	—	—	—	—	—	—	—	—
F7	PTA17	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N

Table continues on the next page...

176 VFBGA	Pin Name	Drive strength	Default status after POR	Pullup/ Pulldown enable after POR	Pullup/ pulldown selection after POR	Slew rate after POR	Passive pin filter after POR	Open drain enable at reset	Open drain enable control	Pin interrupt	Fast capability	Fast high drive
D8	PTA18	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
D7	PTA19	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
C7	PTA20	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
B7	PTA21	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
B6	PTA22/ LLWU_ P2	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
E6	PTA23	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
D6	PTA24	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
B5	PTA25	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
A5	PTA26	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
A3	PTA27	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
A2	PTA28	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
A13[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
E3	VDDIO1	—	—	—	—	—	—	—	—	—	—	—
A1	PTA30/ LLWU_ P3	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
C4	PTA31	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
B3	PTB0	ND	Hi-Z	N	PD	FS	N	N	Y	Y	Y	N
C3	PTB1/ LLWU_ P4	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
B1	PTB2/ LLWU_ P5	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N
B14	VSS	—	—	—	—	—	—	—	—	—	—	—
B15	VSS	—	—	—	—	—	—	—	—	—	—	—
B16	VSS	—	—	—	—	—	—	—	—	—	—	—
C5[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
C13[1]	VSS	—	—	—	—	—	—	—	—	—	—	—

Table continues on the next page...

176 VFBGA	Pin Name	Drive strength	Default status after POR	Pullup/ Pulldown enable after POR	Pullup/ pulldown selection after POR	Slew rate after POR	Passive pin filter after POR	Open drain enable at reset	Open drain enable control	Pin interrupt	Fast capability	Fast high drive
C15[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
C16[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
D9	VSS	—	—	—	—	—	—	—	—	—	—	—
D15	VSS	—	—	—	—	—	—	—	—	—	—	—
F16[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
H8[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
H10[1]	VSS	—	—	—	—	—	—	—	—	—	—	—
K8	VSS	—	—	—	—	—	—	—	—	—	—	—
N14	VDD_CORE	—	—	—	—	—	—	—	—	—	—	—
R15[1]	VSSA	—	—	—	—	—	—	—	—	—	—	—
T2	VDD_DCDC	—	—	—	—	—	—	—	—	—	—	—
B2	PTA30/ LLWU_P3	ND	Hi-Z	N	PD	FS	N	N	Y	Y	N	N

1. Optional, can be left as NC.

Properties	Abbreviation	Descriptions
Driver strength	ND	Normal drive
	HD	High drive
Default status after POR	Hi-Z	High impendence
	H	High level
	L	Low level
Pullup/ pulldown Enable after POR	Y	Enabled
	N	Disabled
Pullup/ pulldown selection after POR	PU	Pullup
	PD	Pulldown
Slew rate after POR	FS	Fast slew rate

Table continues on the next page...

	SS	Slow slew rate
Passive Pin Filter after POR	N	Disabled
	Y	Enabled
Open drain	N	Disabled[1]
	Y	Enabled
Pin interrupt	Y	Yes
Fast capability	N	Not support fast capability
	Y	Support fast capability
Fast high drive	N	Not support fast high drive
	Y	Support fast high drive

1. When an LPI2C module is enabled and a pin is functional for LPI2C, this pin is (pseudo-) open drain enabled. When an LPUART module is enabled and a pin is functional for LPUART, this pin is (pseudo-) open drain configurable.

3.3 Module Signal Description Tables

The following sections correlate the chip-level signal name with the signal name used in the module's chapter. They also briefly describe the signal function and direction.

3.3.1 Core Modules

Table 17. JTAG ARM Signal Descriptions

Chip signal name	Module signal name	Description	I/O
JTAG_TMS	TMS	Test Mode Select	Input
JTAG_TCLK	TCK	Test Clock	Input
JTAG_TDI	TDI	Test Data In	Input
JTAG_TDO	TDO	Test Data Out	Output

Table 18. RISC-V core JTAG Signal Descriptions

Chip signal name	Module signal name	Description	I/O
RV_JTAG_TMS	TMS	Test Mode Select	Input
RV_JTAG_TCLK	TCK	Test Clock	Input
RV_JTAG_TDI	TDI	Test Data In	Input
RV_JTAG_TDO	TDO	Test Data Out	Output

Table 19. SWD Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SWD_DIO	SWD_DIO	Serial Wire Data Input/Output. The SWD_DIO pin is used by an external debug tool for communication and device control. This pin is pulled up internally.	Input / Output
SWD_CLK	SWD_CLK	Serial Wire Clock. This pin is the clock for debug logic when in the Serial Wire Debug mode. This pin is pulled down internally.	Input
SWD_SWO	SWD_SWO	Trace output over a single pin	Output

Table 20. TPIU Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TRACE_CLKOUT	TRACECLK	Trace clock output from the ARM CoreSight debug block	O
TRACE_D[3:2]	TRACEDATA	Trace output data from the ARM CoreSight debug block used for 5-pin interface	O
TRACE_D[1:0]	TRACEDATA	Trace output data from the ARM CoreSight debug block used for both 5-pin and 3-pin interfaces	O

3.3.2 System Modules

Table 21. System Signal Descriptions

Chip signal name	Module signal name	Description	I/O
NMI_b	—	Non-maskable interrupt **NOTE:** Driving the $\overline{\text{NMI}}$ signal low forces a non-maskable interrupt, if the $\overline{\text{NMI}}$ function is selected on the corresponding pin.	I
RESET_b	—	Reset bi-directional signal	I/O
VDD_CORE	—	MCU power	I
VDDIO1	—	I/O rings power	I
VDDIO2	—	I/O rings power	I
VDD_RF	—	Radio power supply	I
VSS	—	MCU ground	I
VSSA	—	Analog ground	I

Table 22. EWM Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EWM_IN	EWM_in	EWM input for safety status of external safety circuits. The polarity of EWM_in is programmable using the EWM_CTRL[ASSIN] bit. The default polarity is active-low.	I
EWM_OUT_b	$\overline{\text{EWM\_out}}$	EWM reset out signal	O

Table 23. LLWU0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LLWU_Pn (n=[31:0]	LLWU_Pn (n=[31:0]	External Pin Wakeup inputs	I

3.3.3 Memories and Memory Interfaces

Table 24. FlexBus Signal Descriptions

Chip signal name	Module signal name	Description	I/O
FB_CLKOUT	FB_CLK	FlexBus Clock Output	O
FB_A[23:16]	FB_A[23:16]	This is the address and data bus	I/O
FB_AD[31:0]	FB_ADn	This is the address and data bus, FB_AD. The number of byte lanes carrying the data is determined by the port size associated with the matching chip-select. The full 32-bit address is driven on the first clock of a bus cycle (address phase). After the first clock, the data is driven on the bus (data phase). During the data phase, the address is driven on the pins not used for data. For example, in 16-bit mode, the lower address is driven on FB_AD15–FB_AD0, and in 8-bit mode, the lower address is driven on FB_AD23–FB_AD0.	I/O
FB_CSn_b (n=[5:0])	$\overline{\text{FB_CS}}$n (n=[5:0])	General Purpose Chip-Selects—Indicate which external memory or peripheral is selected. A particular chip-select is asserted when the transfer address is within the external memory's or peripheral's address space, as defined in CSAR[BA] and CSMR[BAM].	O
FB_BE31_24_b FB_BE23_16_b FB_BE15_8_b FB_BE7_0_b	$\overline{\text{FB\_BE\_31\_24}}$, $\overline{\text{FB\_BE\_23\_16}}$, $\overline{\text{FB\_BE\_15\_8}}$, $\overline{\text{FB\_BE\_7\_0}}$	Byte Enables—Indicate that data is to be latched or driven onto a specific byte lane of the data bus. CSCR[BEM] determines if these signals are asserted on reads and writes or on writes only. For external SRAM or flash devices, the FB_BE outputs should be connected to individual byte strobe signals.	O
FB_OE_b	$\overline{\text{FB\_OE}}$	Output Enable—Sent to the external memory or peripheral to enable a read transfer. This signal is asserted during read accesses only when a chip-select matches the current address decode.	O

Table continues on the next page...

Table 24. FlexBus Signal Descriptions (continued)

Chip signal name	Module signal name	Description	I/O
FB_RW_b	FB_R$\overline{W}$	Read/Write—Indicates whether the current bus operation is a read operation (FB_R/W high) or a write operation (FB_R/$\overline{W}$ low).	O
FB_TS_b	$\overline{FB\_TS}$	Transfer Start—Indicates that the chip has begun a bus transaction and that the address and attributes are valid.	O
FB_ALE	FB_ALE	Address Latch Enable—Indicates when the address is being driven on the FB_A bus (inverse of $\overline{FB\_TS}$).	O
FB_TSIZn (n=[1:0])	FB_TSIZn (n=[1:0])	Transfer Size—Indicates (along with FB_TBST) the data transfer size of the current bus operation. The interface supports 8-, 16-, and 32-bit operand transfers and allows accesses to 8-, 16-, and 32-bit data ports.	O
$\overline{FB\_TA\_b}$	$\overline{FB\_TA}$	Transfer Acknowledge—Indicates that the external data transfer is complete. When $\overline{FB\_TA}$ is asserted during a read transfer, FlexBus latches the data and then terminates the transfer. When $\overline{FB\_TA}$ is asserted during a write transfer, the transfer is terminated.	I
FB_TBST_b	$\overline{FB\_TBST}$	Transfer Burst—Indicates that a burst transfer is in progress as driven by the chip. A burst transfer can be 2 to 16 beats depending on FB_TSIZ1–FB_TSIZ0 and the port size.	O

3.3.4 Clock Modules

Table 25. RTC OSC Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL32	EXTAL32	32.768 kHz oscillator input	I
XTAL32	XTAL32	32.768 kHz oscillator output	O

Table 26. Radio OSC Signal Descriptions

Chip signal name	Module signal name	Description	I/O
XTAL_RF	RF XTAL	26 or 32 MHz oscillator output	O
EXTAL_RF	RF EXTAL	26 or 32 MHz oscillator input	I
RF0_EXT_OSC_EN	RF_EXT_OSC_EN	Internal request to turn on an External Osc for use by the internal Radio, this can also be a request from the SoC if it is using the RF Osc as it's clock.	O
RF0_RFOSC_EN	RF_INT_OSC_EN	External request to turn on the Radio's internal RF Osc. The Osc will be present on the XTAL_OUT pin if the RF Osc XTAL_OUT buffer is enabled by writing the Radio XTAL_OUT_BUF_EN bit in the RSIM ANA_TEST register.	I

Table continues on the next page...

Table 26. Radio OSC Signal Descriptions (continued)

Chip signal name	Module signal name	Description	I/O
RF_CLKOUT	XTAL_OUT	26 MHz/32 MHz reference clock output	O

3.3.5 Communication Interfaces

Table 27. EMVSIM Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EMVSIM0_CLK	EMVSIM_SCLK	Card Clock. Clock to Smart Card.	O
EMVSIM0_RST	EMVSIM_SRST	Card Reset. Reset signal to Smart Card	O
EMVSIM0_VCCEN	EMVSIM_VCC_EN	Card Power Enable. This signal controls the power to Smart Card	O
EMVSIM0_IO	EMVSIM_IO	Card Data Line. Bi-directional data line.	I/O
EMVSIM0_PD	EMVSIM_PD	Card Presence Detect. Signal indicating presence or removal of card	I

Table 28. USB FS Signal Descriptions

Chip signal name	Module signal name	Description	I/O
USB0_DM	usb_dm	USB D- analog data signal on the USB bus.	I/O
USB0_DP	usb_dp	USB D+ analog data signal on the USB bus.	I/O
USB_SOF_OUT	—	USB start of frame signal. Can be used to make the USB start of frame available for external synchronization.	O
USB0_VSS	—	V_{SS} for USB0	—

Table 29. USB VREG Signal Descriptions

Chip signal name	Module signal name	Description	I/O
VOUT33	reg33_out	Regulator output voltage	O
VREGIN	vreg_in1	Unregulated power supply	I

Table 30. LPSPI0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SPI0_SCK	SCK	Serial clock. Input in slave mode, output in master mode.	I/O

Table continues on the next page...

Table 30. LPSPI0 Signal Descriptions (continued)

Chip signal name	Module signal name	Description	I/O
SPI0_PCS0	PCS[0]	Peripheral Chip Select. Input in slave mode, output in master mode.	I/O
SPI0_PCS1	PCS[1]	Peripheral Chip Select or Host Request. Host Request pin is selected when HREN=1 and HRSEL=0. Input in either slave mode or when used as Host Request, output in master mode.	I/O
SPI0_PCS2	PCS[2]	Peripheral Chip Select or data pin 2 during quad-data transfers. Input in slave mode, output in master mode, input in quad-data receive transfers, output in quad-data transmit transfers.	I/O
SPI0_PCS3	PCS[3]	Peripheral Chip Select or data pin 3 during quad-data transfers. Input in slave mode, output in master mode, input in quad-data receive transfers, output in quad-data transmit transfers.	I/O
SPI0_SOUT	SOUT	Serial Data Output. Can be configured as serial data input signal. Used as data pin 0 in quad-data and dual-data transfers.	I/O
SPI0_SIN	SIN	Serial Data Input. Can be configured as serial data output signal. Used as data pin 1 in quad-data and dual-data transfers.	I/O

Table 31. LPSPI1 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SPI1_SCK	SCK	Serial clock. Input in slave mode, output in master mode.	I/O
SPI1_PCS0	PCS[0]	Peripheral Chip Select. Input in slave mode, output in master mode.	I/O
SPI1_PCS1	PCS[1]	Peripheral Chip Select or Host Request. Host Request pin is selected when HREN=1 and HRSEL=0. Input in either slave mode or when used as Host Request, output in master mode.	I/O
SPI1_PCS2	PCS[2]	Peripheral Chip Select or data pin 2 during quad-data transfers. Input in slave mode, output in master mode, input in quad-data receive transfers, output in quad-data transmit transfers.	I/O
SPI1_PCS3	PCS[3]	Peripheral Chip Select or data pin 3 during quad-data transfers. Input in slave mode, output in master mode, input in quad-data receive transfers, output in quad-data transmit transfers.	I/O
SPI1_SOUT	SOUT	Serial Data Output. Can be configured as serial data input signal. Used as data pin 0 in quad-data and dual-data transfers.	I/O
SPI1_SIN	SIN	Serial Data Input. Can be configured as serial data output signal. Used as data pin 1 in quad-data and dual-data transfers.	I/O

Table 32. LPSPI2 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SPI2_SCK	SCK	Serial clock. Input in slave mode, output in master mode.	I/O

Table continues on the next page...

Table 32. LPSPI2 Signal Descriptions (continued)

Chip signal name	Module signal name	Description	I/O
SPI2_PCS0	PCS[0]	Peripheral Chip Select. Input in slave mode, output in master mode.	I/O
SPI2_PCS1	PCS[1]	Peripheral Chip Select or Host Request. Host Request pin is selected when HREN=1 and HRSEL=0. Input in either slave mode or when used as Host Request, output in master mode.	I/O
SPI2_PCS2	PCS[2]	Peripheral Chip Select or data pin 2 during quad-data transfers. Input in slave mode, output in master mode, input in quad-data receive transfers, output in quad-data transmit transfers.	I/O
SPI2_PCS3	PCS[3]	Peripheral Chip Select or data pin 3 during quad-data transfers. Input in slave mode, output in master mode, input in quad-data receive transfers, output in quad-data transmit transfers.	I/O
SPI2_SOUT	SOUT	Serial Data Output. Can be configured as serial data input signal. Used as data pin 0 in quad-data and dual-data transfers.	I/O
SPI2_SIN	SIN	Serial Data Input. Can be configured as serial data output signal. Used as data pin 1 in quad-data and dual-data transfers.	I/O

Table 33. LPSPI3 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SPI3_SCK	SCK	Serial clock. Input in slave mode, output in master mode.	I/O
SPI3_PCS0	PCS[0]	Peripheral Chip Select. Input in slave mode, output in master mode.	I/O
SPI3_PCS1	PCS[1]	Peripheral Chip Select or Host Request. Host Request pin is selected when HREN=1 and HRSEL=0. Input in either slave mode or when used as Host Request, output in master mode.	I/O
SPI3_PCS2	PCS[2]	Peripheral Chip Select or data pin 2 during quad-data transfers. Input in slave mode, output in master mode, input in quad-data receive transfers, output in quad-data transmit transfers.	I/O
SPI3_PCS3	PCS[3]	Peripheral Chip Select or data pin 3 during quad-data transfers. Input in slave mode, output in master mode, input in quad-data receive transfers, output in quad-data transmit transfers.	I/O
SPI3_SOUT	SOUT	Serial Data Output. Can be configured as serial data input signal. Used as data pin 0 in quad-data and dual-data transfers.	I/O
SPI3_SIN	SIN	Serial Data Input. Can be configured as serial data output signal. Used as data pin 1 in quad-data and dual-data transfers.	I/O

Table 34. LPI2C0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
I2C0_SCL	SCL	LPI2C clock line. In 4-wire mode, this is the SCL input pin.	I/O

Table continues on the next page...

Table 34. LPI2C0 Signal Descriptions (continued)

Chip signal name	Module signal name	Description	I/O
I2C0_SDA	SDA	LPI2C data line. In 4-wire mode, this is the SDA input pin.	I/O
LPI2C0_HREQ	HREQ	Host request, can initiate an LPI2C master transfer if asserted and the I2C bus is idle.	I
LPI2C0_SCLS	SCLS	Secondary I2C clock line. In 4-wire mode, this is the SCLS output pin. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SCL pin.	I/O
LPI2C0_SDAS	SDAS	Secondary I2C data line. In 4-wire mode, this is the SDAS output pin. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SDA pin.	I/O

Table 35. LPI2C1 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
I2C1_SCL	SCL	LPI2C clock line. In 4-wire mode, this is the SCL input pin.	I/O
I2C1_SDA	SDA	LPI2C data line. In 4-wire mode, this is the SDA input pin.	I/O
LPI2C1_HREQ	HREQ	Host request, can initiate an LPI2C master transfer if asserted and the I2C bus is idle.	I
LPI2C1_SCLS	SCLS	Secondary I2C clock line. In 4-wire mode, this is the SCLS output pin. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SCL pin.	I/O
LPI2C1_SDAS	SDAS	Secondary I2C data line. In 4-wire mode, this is the SDAS output pin. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SDA pin.	I/O

Table 36. LPI2C2 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
I2C2_SCL	SCL	LPI2C clock line. In 4-wire mode, this is the SCL input pin.	I/O
I2C2_SDA	SDA	LPI2C data line. In 4-wire mode, this is the SDA input pin.	I/O
LPI2C2_HREQ	HREQ	Host request, can initiate an LPI2C master transfer if asserted and the I2C bus is idle.	I
LPI2C2_SCLS	SCLS	Secondary I2C clock line. In 4-wire mode, this is the SCLS output pin. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SCL pin.	I/O
LPI2C2_SDAS	SDAS	Secondary I2C data line. In 4-wire mode, this is the SDAS output pin. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SDA pin.	I/O

Table 37. LPI2C3 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
I2C3_SCL	SCL	LPI2C clock line. In 4-wire mode, this is the SCL input pin.	I/O
I2C3_SDA	SDA	LPI2C data line. In 4-wire mode, this is the SDA input pin.	I/O
LPI2C3_HREQ	HREQ	Host request, can initiate an LPI2C master transfer if asserted and the I2C bus is idle.	I
LPI2C3_SCLS	SCLS	Secondary I2C clock line. In 4-wire mode, this is the SCLS output pin. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SCL pin.	I/O
LPI2C3_SDAS	SDAS	Secondary I2C data line. In 4-wire mode, this is the SDAS output pin. If LPI2C master/slave are configured to use separate pins, this the LPI2C slave SDA pin.	I/O

Table 38. LPUART0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPUART0_CTS	CTS	Clear to Send.	I
LPUART0_RTS	RTS	Request to send.	O
LPUART0_TX	TXD	Transmit data. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data.	I/O
LPUART0_RX	RXD	Receive data.	I

Table 39. LPUART1 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPUART1_CTS	CTS	Clear to Send.	I
LPUART1_RTS	RTS	Request to send.	O
LPUART1_TX	TXD	Transmit data. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data.	I/O
LPUART1_RX	RXD	Receive data.	I

Table 40. LPUART2 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPUART2_CTS	CTS	Clear to Send.	I
LPUART2_RTS	RTS	Request to send.	O

Table continues on the next page...

Table 40. LPUART2 Signal Descriptions (continued)

Chip signal name	Module signal name	Description	I/O
LPUART2_TX	TXD	Transmit data. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data.	I/O
LPUART2_RX	RXD	Receive data.	I

Table 41. LPUART3 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPUART3_CTS	CTS	Clear to Send.	I
LPUART3_RTS	RTS	Request to send.	O
LPUART3_TX	TXD	Transmit data. This pin is normally an output, but is an input (tristated) in single wire mode whenever the transmitter is disabled or transmit direction is configured for receive data.	I/O
LPUART3_RX	RXD	Receive data.	I

Table 42. SDHC Signal Descriptions

Chip signal name	Module signal name	Description	I/O
SDHC0_DCLK	CLK	Clock for MMC/SD/SDIO card	O
SDHC0_CMD	CMD	CMD line connect to card	I/O
SDHC0_D0	DAT0	DAT0 line in all modes. Also used to detect busy state	I/O
SDHC0_D1	DAT1	DAT1 line in 4/8-bit mode.Also used to detect interrupt in 1/4-bit mode	I/O
SDHC0_D2	DAT2	DAT2 line or Read Wait in 4-bit mode. Read Wait in 1-bit mode	I/O
SDHC0_D3	DAT3	DAT3 line in 4/8-bit mode or configured as card detection pin. May be configured as card detection pin in 1-bit mode	I/O
SDHC0_D4	DAT4	DAT4 line in 8-bit mode. Not used in other modes	I/O
SDHC0_D5	DAT5	DAT5 line in 8-bit mode. Not used in other modes	I/O
SDHC0_D6	DAT6	DAT6 line in 8-bit mode. Not used in other modes	I/O
SDHC0_D7	DATA7	DAT7 line in 8-bit mode.Not used in other modes	I/O

Table 43. I^2S0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
I2S0_TX_BCLK	SAI_TX_BCLK	Transmit Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O

Table continues on the next page...

Table 43. I²S0 Signal Descriptions (continued)

Chip signal name	Module signal name	Description	I/O
I2S0_TX_FS	SAI_TX_SYNC	Transmit Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
I2S0_TX_Dn n=[1:0]	SAI_TX_DATA[1:0]	Transmit Data. The transmit data is generated synchronously by the bit clock and is tristated whenever not transmitting a word.	O
I2S0_RX_BCLK	SAI_RX_BCLK	Receive Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O
I2S0_RX_FS	SAI_RX_SYNC	Receive Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
I2S0_RX_Dn	SAI_RX_DATA[1:0]	Receive Data. The receive data is sampled synchronously by the bit clock.	I
I2S0_MCLK	MCLK_EN	Audio Master Clock.	I

Table 44. FlexIO Signal Descriptions

Chip signal name	Module signal name	Description	I/O
FXIO0_Dn (n=[31:0]	FXIO_Dn (n=[31:0]	Bidirectional FlexIO Shifter and Timer pin inputs/outputs	I/O

3.3.6 Analog

Table 45. LPADC0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPADC0_SE[23:0]	CHnA (n=[23:0]	A-side Analog Channel Inputs	I
VDDA	VDDA	Analog Power Supply	I
VSSA	VSSA	Analog Ground	I

Table 46. LPCMP0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPCMP0_IN[5:0]	IN[5:0]	Analog voltage inputs	I
LPCMP0_OUT	CMPO	Comparator output	O

Table 47. LPCMP1 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPCMP1_IN[5:0]	IN[5:0]	Analog voltage inputs	I
LPCMP1_OUT	CMPO	Comparator output	O

Table 48. LPDAC0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
DAC0_OUT	—	DAC output	O

Table 49. VREF Signal Descriptions

Chip signal name	Module signal name	Description	I/O
VREF_OUT	VREF_OUT	Internally-generated Voltage Reference output	O

3.3.7 Human-Machine Interfaces (HMI)

Table 50. GPIO Signal Descriptions

Chip signal name	Module signal name	Description	I/O
PTA[31:0][1]	PORTA31–PORTA0	General-purpose input/output	I/O
PTB[31:0][1]	PORTB31–PORTB0	General-purpose input/output	I/O
PTC[31:0][1]	PORTC31–PORTC0	General-purpose input/output	I/O
PTD[31:0][1]	PORTD31–PORTD0	General-purpose input/output	I/O
PTE[31:0][1]	PORTE31–PORTE0	General-purpose input/output	I/O

1. The available GPIO pins depends on the specific package. See the signal multiplexing section for which exact GPIO signals are available.

3.3.8 Timer Modules

Table 51. LPTMR0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPTMR0_ALT[3:1]	LPTMR_ALTn,n=[3:1]	Pulse Counter Input - The LPTMR can select one of the input pins to be used in Pulse Counter mode.	I

Table 52. LPTMR1 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPTMR1_ALT[3:1]	LPTMR_ALTn,n=[3:1]	Pulse Counter Input - The LPTMR can select one of the input pins to be used in Pulse Counter mode.	I

Table 53. LPTMR2 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
LPTMR2_ALT[3:1]	LPTMR_ALTn,n=[3:1]	Pulse Counter Input - The LPTMR can select one of the input pins to be used in Pulse Counter mode.	I

Table 54. TPM0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TPM0_CH[5:0]	TPM_CHn (n=[5:0])	TPM channel. A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O
TPM0_CLKIN	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the counter on every rising edge synchronized to the counter clock.	I

Table 55. TPM1 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TPM1_CH[1:0]	TPM_CHn (n=[1:0])	TPM channel. A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O
TPM1_CLKIN	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the counter on every rising edge synchronized to the counter clock.	I

Table 56. TPM2 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TPM2_CH[5:0]	TPM_CHn (n=[5:0])	TPM channel. A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O
TPM2_CLKIN	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the counter on every rising edge synchronized to the counter clock.	I

Table 57. TPM3 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TPM3_CH[1:0]	TPM_CHn (n=[1:0])	TPM channel. A TPM channel pin is configured as output when configured in an output compare or PWM mode and the TPM counter is enabled, otherwise the TPM channel pin is an input.	I/O
TPM3_CLKIN	TPM_EXTCLK	External clock. TPM external clock can be selected to increment the counter on every rising edge synchronized to the counter clock.	I

Table 58. TPM0 Signal Descriptions

Chip signal name	Module signal name	Description	I/O
EXTAL32	EXTAL32	32.768 kHz oscillator input	I
XTAL32	XTAL32	32.768 kHz oscillator output	O
RTC_CLKOUT	RTC_CLKOUT	Prescaler square-wave output or 32kHz crystal clock	O
RTC_WAKEUP_b	$\overline{\text{RTC\_WAKEUP}}$	Active low wakeup for external device	O

3.3.9 Security Modules

Table 59. Tamper Detect Signal Descriptions

Chip signal name	Module signal name	Description	I/O
TAMPER[3:0] [1]	RTC_TAMPER[3:0]	Tamper pin input	I

1. The TAMPER signals have dedicated pins and are not included in the JTAG boundary scan. TAMPER0 is an exception because it is priority muxed with the RTC_WAKEUP_b function. If TAMPER0 is enabled as either an input or output, the RTC_WAKEUP_b function is disabled. The RTC_WAKEUP_b pin can be configured to assert on a Tamper Detect, if the RTC enables the DryIce tamper detect interrupt.

3.4 Pinouts diagram

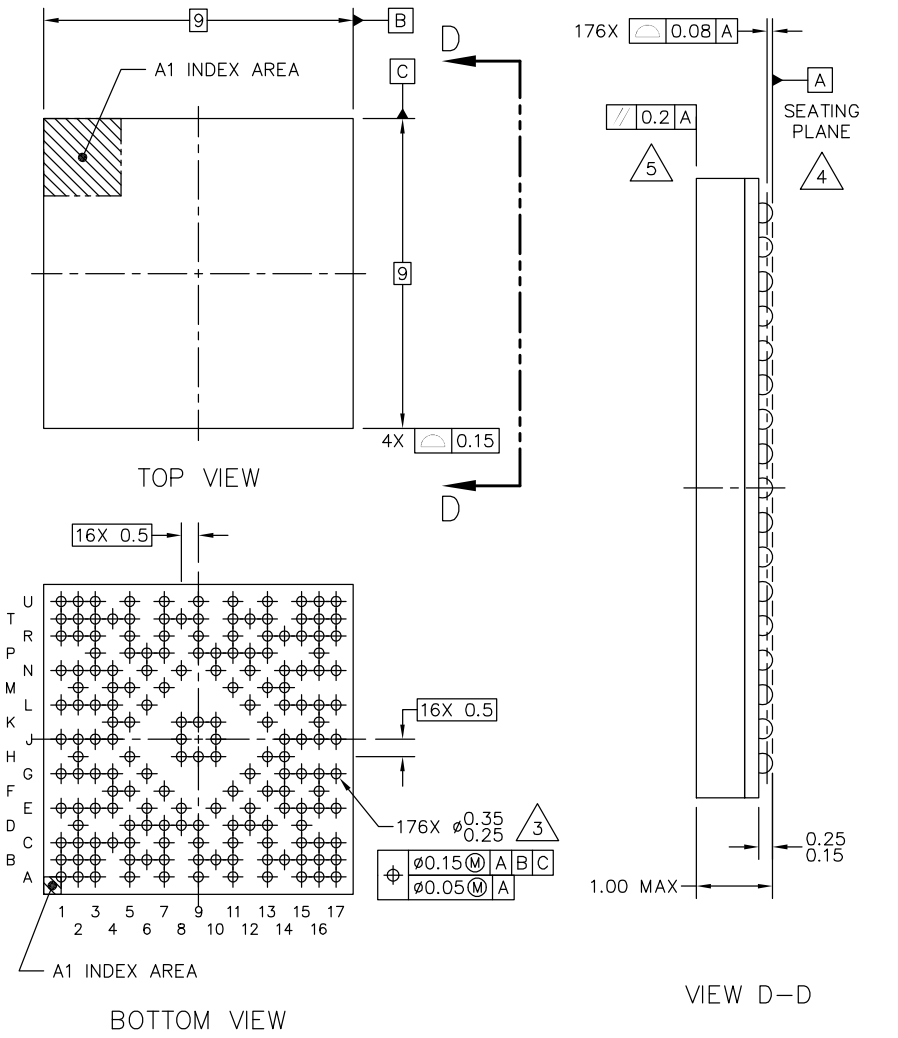
The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17A	
A	PTA30/LLWU_P3	PTA28	PTA27	NC	PTA26	NC	PTA15	NC	PTA10	NC	XTAL_RF	NC	VSS	NC	ANT	GANT	VSS	A
B	PTB2/LLWU_P5	PTA30/LLWU_P3	PTB0	NC	PTA25	PTA22/LLWU_P2	PTA21	NC	PTA4	PTA0	EXTAL_RF	NC	VDD_RF	VSS	VSS	VSS	VDD_RF	B
C	PTB3	PTB4/LLWU_P6	PTB1/LLWU_P4	PTA31	VSS	NC	PTA20	NC	VDDIO1	NC	RF_CLKOUT	NC	VSS	NC	VSS	VSS	VDD_RF	C
D	NC	PTB5	NC	NC	VSS	PTA24	PTA19	PTA18	VSS	NC	PTA3	RESET_b	VDDIO2	NC	VSS	NC	NC	D
E	PTB6/LLWU_P7	PTB7/LLWU_P8	VDDIO1	VDDIO1	NC	PTA23	NC	PTA14	NC	PTA9	NC	PTA1/LLWU_P0	NC	VSS	VSS	EXTAL32	XTAL32	E
F	NC	NC	NC	PTB9	PTB8/LLWU_P9	NC	PTA17	NC	NC	NC	PTA2/LLWU_P1	NC	TAMPER1/RTC_CLKOUT	TAMPER0/RTC_WAKEUP	NC	VSS	NC	F
G	PTB15	PTB14	PTB13	PTB12	NC	PTB11	NC	NC	NC	NC	NC	TAMPER2	NC	PTE28	PTE29	VBAT	PTE30	G
H	NC	PTB18	NC	NC	PTB16/LLWU_P10	NC	NC	VSS	VDD_CORE	VSS	NC	NC	TAMPER3	PTE27	NC	NC	NC	H
J	PTB20/LLWU_P11	PTB21	VDDIO1	VSS	NC	NC	NC	VDD_CORE	NC	VDDIO1	NC	NC	NC	VSS	VDDIO2	PTE22	PTE21	J
K	NC	NC	NC	PTB19	PTB17	NC	NC	VSS	VDDIO1	VSS	NC	NC	PTE18	NC	NC	PTE19	NC	K
L	PTB22/LLWU_P12	PTB24	PTB29	PTB26	NC	PTB25/LLWU_P13	NC	NC	NC	NC	NC	PTE12/LLWU_P26	NC	PTE16	PTE17	PTE14	PTE15	L
M	NC	PTC1	NC	PTB28/LLWU_P14	PTB30	NC	PTB31	NC	NC	NC	PTE4	NC	PTE10/LLWU_P25	PTE11	NC	NC	NC	M
N	PTC0	PTC7/LLWU_P15	VSS	USB0_VSS	NT	PTC29	NT	PTD4	NT	PTD5	NT	PTE3/LLWU_P22	NT	VDD_CORE	VDD_CORE	PTE9/LLWU_P24	PTE13	N
P	NC	NC	PTC8	NC	VDDIO1	PTC27	PTD1	NC	VSS	PTD7	PTD10/LLWU_P20	PTE2	VSS	NC	NC	PTE8/LLWU_P23	NC	P
R	PTC9/LLWU_P16	PTC10	PTC12/LLWU_P18	NC	VDDIO1	NC	PTC30	NC	VDDIO1	NC	PTD11	NC	VSS	PTE0	VSSA	PTE1/LLWU_P21	PTE5	R
T	PTC11/LLWU_P17	VDD_DCDC	VOUT_RF	LN	VOUT_CORE	NC	PTD0	PTD3	PTD8/LLWU_P19	NC	USB0_DP	USB0_DM	VOUT33	NC	VREF_OUT	VSSA	DAC0_OUT	T
U	VDD_DCDC	LP	GND	NC	PTC28	NC	PTD2	NC	PTD6	NC	PTD9	NC	VREGIN	NC	VDDA	VREFH	VREFL	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 7. VFBGA Pinout Diagram

3.5 Package dimensions

The following figures show the dimensions of the package options for the devices supported by this document.



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURED PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.

Figure 8. 176 VFBGA package dimension

4 Electrical characteristics

4.1 Terminology and guidelines

4.1.1 Definitions

Key terms are defined in the following table:

Term	Definition
Rating	A minimum or maximum value of a technical characteristic that, if exceeded, may cause permanent chip failure: • *Operating ratings* apply during operation of the chip. • *Handling ratings* apply when the chip is not powered. **NOTE:** The likelihood of permanent chip failure increases rapidly as soon as a characteristic begins to exceed one of its operating ratings.
Operating requirement	A specified value or range of values for a technical characteristic that you must guarantee during operation to avoid incorrect operation and possibly decreasing the useful life of the chip
Operating behavior	A specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions
Typical value	A specified value for a technical characteristic that: • Lies within the range of values specified by the operating behavior • Is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions **NOTE:** Typical values are provided as design guidelines and are neither tested nor guaranteed.

4.1.2 Examples

Operating rating:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	–0.3	1.2	V

Operating requirement:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

Operating behavior that includes a *typical value*:

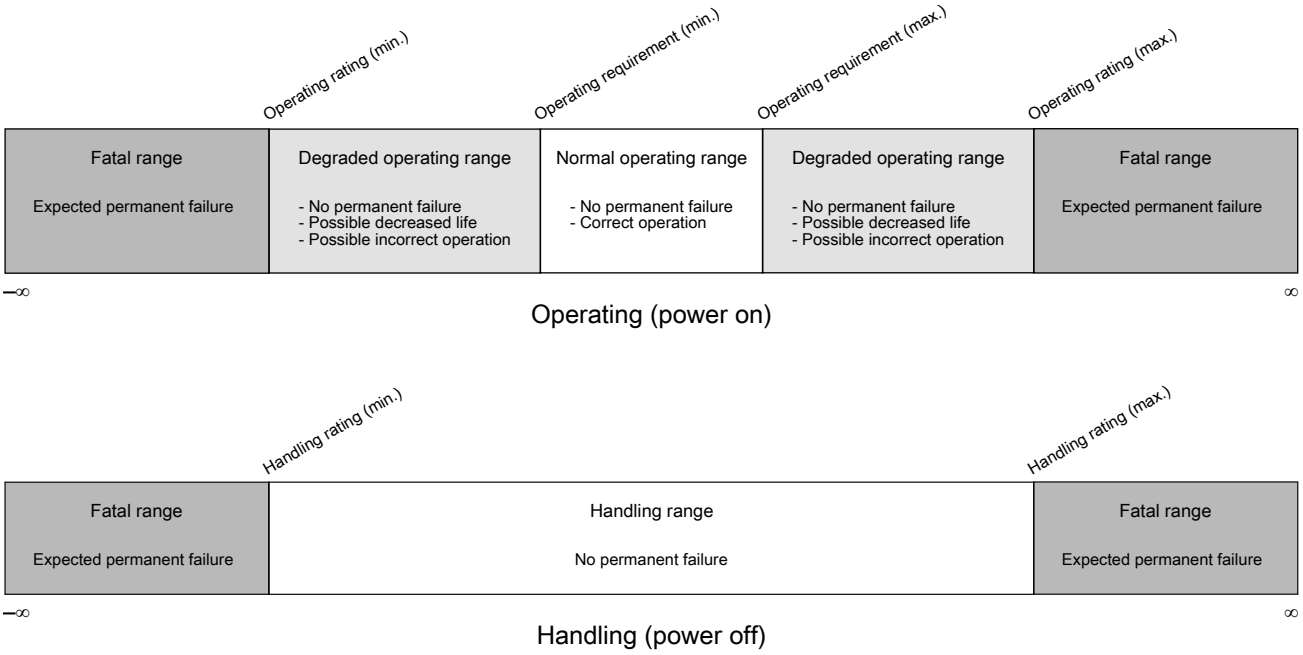
Symbol	Description	Min.	Typ.	Max.	Unit
I_{WP}	Digital I/O weak pullup/pulldown current	10	70	130	µA

4.1.3 Typical-value conditions

Typical values assume you meet the following conditions (or other conditions as specified):

Symbol	Description	Value	Unit
T_A	Ambient temperature	25	°C
V_{DDIOx}	Supply voltage	3.3	V

4.1.4 Relationship between ratings and operating requirements



4.1.5 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

4.2 Ratings

4.2.1 Thermal handling ratings

Table 60. Thermal handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
T_{STG}	Storage temperature	–55	150	°C	1
T_{SDR}	Solder temperature, lead-free	—	260	°C	2

1. Determined according to JEDEC Standard JESD22-A103, *High Temperature Storage Life*.

2. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2.2 Moisture handling ratings

Table 61. Moisture handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
MSL	Moisture sensitivity level	—	3	—	1

1. Determined according to IPC/JEDEC Standard J-STD-020, *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*.

4.2.3 ESD handling ratings

Table 62. ESD handling ratings

Symbol	Description	Min.	Max.	Unit	Notes
V_{HBM}	Electrostatic discharge voltage, human body model	–2000	+2000	V	1
V_{CDM}	Electrostatic discharge voltage, charged-device model	–500	+500	V	2
I_{LAT}	Latch-up current at ambient temperature of 105 °C	–100	+100	mA	3

1. Determined according to JEDEC Standard JESD22-A114, *Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)*.
2. Determined according to JEDEC Standard JESD22-C101, *Field-Induced Charged-Device Model Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components*.
3. Determined according to JEDEC Standard JESD78, *IC Latch-Up Test*.

4.2.4 Voltage and current operating ratings

Table 63. Voltage and current operating ratings

Symbol	Description	Min.	Max.	Unit	Note
V_{DD_DCDC}	MCU regulator input	-0.3	3.6	V	
V_{DDIOx}	Digital supply voltage	-0.3	3.6	V	
V_{DD_CORE}	Internal digital logic supply voltage	-0.3	1.47	V	
V_{DDA}	Analog supply voltage	V_{DDIO} - 0.3	V_{DDIO} + 0.3	V	1
V_{DD_RF}	RF supply voltage	-0.3	3.6	V	
V_{BAT}	RTC supply voltage	-0.3	3.6	V	
I_{DD}	Digital supply current	—	120	mA	
V_{IO}	IO pin input voltage	-0.3	V_{DDIOx} + 0.3	V	

Table continues on the next page...

Table 63. Voltage and current operating ratings (continued)

Symbol	Description	Min.	Max.	Unit	Note
I_D	Instantaneous maximum current single pin limit (applies to all port pins)	-25	25	mA	
V_{USB_DP}	USB_DP input voltage	-0.3	3.63	V	
V_{USB_DM}	USB_DM input voltage	-0.3	3.63	V	
V_{REGIN}	USB regulator input	-0.3	6	V	

1. The V_{DDIO} here is the Maximum of V_{DDIO1} and V_{DDIO2}.

4.2.4.1 Required Power-On-Reset (POR) Sequencing

- V_{DDIO1} and V_{DD_CORE}

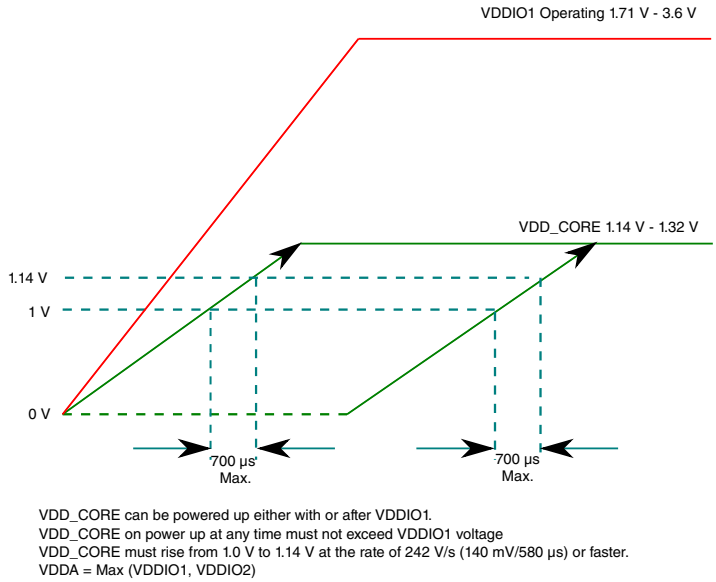
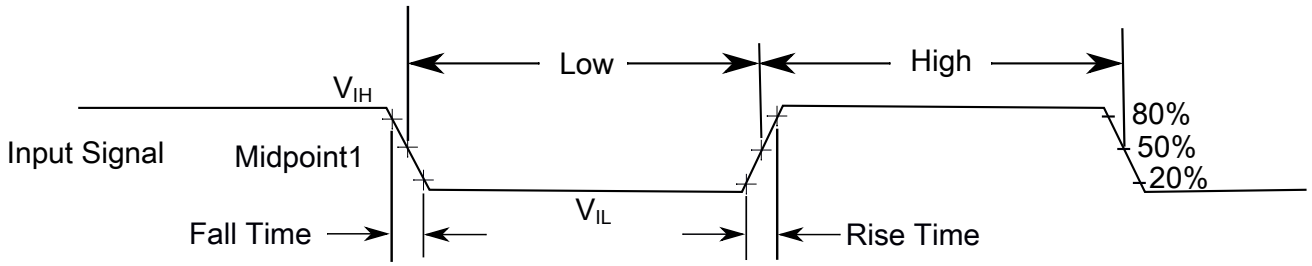


Figure 9. V_{DD_CORE}/ V_{DDIO1} Powering sequence

4.3 General

4.3.1 AC electrical characteristics

Unless otherwise specified, propagation delays are measured from the 50% to the 50% point, and rise and fall times are measured at the 20% and 80% points, as shown in the following figure.



The midpoint is V_{IL} + (V_{IH} - V_{IL}) / 2

Figure 10. Input signal measurement reference

All digital I/O switching characteristics, unless otherwise specified, assume that the output pins have the following characteristics.

- C_L=30 pF loads
- Slew rate disabled
- Normal drive strength

4.3.2 Nonswitching electrical specifications

4.3.2.1 Voltage and current operating requirements

NOTE

The term 'V_{DDIO}' in the following table refers to the associated supply rail (either V_{DDIO1} or V_{DDIO2}) of an input or output.

Table 64. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD_DCDC}(RUN)	Supply of DCDC and IOREG.	2.1	3.6	V	
V_{DD_CORE}(RUN)	Core and digital logic supply voltage for RUN mode	1.14	1.32	V	1
V_{DD_CORE}(HSRUN)	Core and digital logic supply voltage for HSRUN mode	1.33	1.47	V	
V_{DDIO1}	Supply for Ports A, B, C, D and CORELDO	1.71	3.6	V	
V_{DDIO2}	Supply for Port E	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DDIO} - V_{DDA}$	V_{DDIO}-to-V_{DDA} differential voltage	–100	100	mV	2
$V_{SS} - V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{DD_RF}	RF supply voltage	1.45	3.6	V	3

Table continues on the next page...

Table 64. Voltage and current operating requirements (continued)

Symbol	Description	Min.	Max.	Unit	Notes
V_{IH}	Input high voltage • 2.7 V ≤ V_{DDIO} ≤ 3.6 V • 1.71 V ≤ V_{DDIO} ≤ 2.7 V	 0.7 × V_{DDIO} 0.75 × V_{DDIO}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DDIO} ≤ 3.6 V • 1.71 V ≤ V_{DDIO} ≤ 2.7 V	 — —	 0.35 × V_{DDIO} 0.3 × V_{DDIO}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DDIO}	—	V	
I_{ICIO}	IO pin negative DC injection current — single pin • V_{IN} < V_{SS}-0.3V	-5	—	mA	4
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents of 16 contiguous pins • Negative current injection	-25	—	mA	
V_{ODPU}	Open drain pullup voltage level	V_{DDIO}	V_{DDIO}	V	5
V_{RAM}	V_{DD_CORE} voltage required to retain RAM	1.14	—	V	

1. The cores will still execute code in RUN if the core voltage is greater than 1.32 V. However full chip functionality is not guaranteed when in RUN mode and the core voltage is greater than 1.32 V. The core voltage must only be elevated to greater than 1.32 V when transitioning to HSRUN mode.
2. The V_{DDIO} here is the Maximum of V_{DDIO1} and V_{DDIO2}
3. V_{DD_RF} must not be above the V_{DDIO1} to avoid leakage issue.
4. All I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to the corresponding V_{DDIO} supply. If V_{IN} greater than V_{IO_MIN} (= V_{SS}-0.3 V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as R = (V_{IO_MIN} - V_{IN})/|I_{ICIO}|.
5. Open drain outputs must be pulled to whichever supply voltage corresponds to that IO, either VDDIO1 or VDDIO2 as appropriate.

4.3.2.2 HVD, LVD and POR operating requirements

Table 65. V_{DDIO1} supply HVD, LVD and POR Operating Ratings

Characteristic	Symbol	Min	Typ	Max	Unit
High Voltage Detect (High Trip Point)	V_{HVDH}	—	3.72	—	V
High Voltage Detect (Low Trip Point)	V_{HVDL}	—	3.46	—	V
POR re-arm voltage	V_{POR}	0.8	1.1	1.5	V
Falling low-voltage detect threshold -- high range (LVDV=01)	V_{LVDH}	2.48	2.56	2.64	V
Low-voltage warning thresholds -- high range Level 1 falling (LVWV=00)	V_{LVW1} V_{LVW2}	2.62 2.72	2.70 2.80	2.78 2.88	V

Table continues on the next page...

Table 65. V_{DDIO1} supply HVD, LVD and POR Operating Ratings (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
Level 2 falling (LVWV=01)					
Low-voltage inhibit reset/recover hysteresis -- high range	V_{HYS}	—	60	—	mV
Falling low-voltage detect threshold -- low range (LVDV=00)	V_{LVDL}	1.54	1.60	1.66	V
Low-voltage warning thresholds -- low range Level 1 falling (LVWV=00) Level 2 falling (LVWV=01)	V_{LVW1} V_{LVW2}	1.74 1.84	1.80 1.90	1.86 1.96	V
Low-voltage inhibit reset/recover hysteresis -- low range	V_{HYS}	—	40	—	mV
Bandgap voltage reference voltage	V_{BG}	0.97	1.00	1.03	V

NOTE

There is no LVD circuit for VDDIO2 domain

Table 66. Low Voltage Detect of V_{DD_CORE} supply

Characteristic	Symbol	Min	Typ	Max	Unit
Low Voltage Detect of V_{DD_CORE} supply[1]	$V_{LVD\_VDD\_CORE}$	0.95	1	1.08	V

1. There is no High Voltage Detect on V_{DD_CORE}

4.3.2.3 Voltage and current operating behaviors

NOTE

The term 'V_{DDIO}' in the following table refers to the associated supply rail (either V_{DDIO1} or V_{DDIO2}) of an input or output.

Table 67. Voltage and current operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{OH}	Output high voltage — Normal drive pad • 2.7 V ≤ V_{DDIO} ≤ 3.6 V, I_{OH} = –5 mA • 1.71 V ≤ V_{DDIO} ≤ 2.7 V, I_{OH} = –2.5 mA	 V_{DDIO} – 0.5 V_{DDIO} – 0.5		 — —	 V V	1
V_{OH}	Output high voltage — High drive pad • 2.7 V ≤ V_{DDIO} ≤ 3.6 V, I_{OH} = –20 mA • 1.71 V ≤ V_{DDIO} ≤ 2.7 V, I_{OH} = –10 mA	 V_{DDIO} – 0.5		 — —	 V V	1

Table continues on the next page...

Table 67. Voltage and current operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
		V_{DDIO} – 0.5				
I_{OHT}	Output high current total for all ports	—		100	mA	
V_{OL}	Output low voltage — Normal drive pad • 2.7 V ≤ V_{DDIO} ≤ 3.6 V, I_{OL} = 5 mA • 1.71 V ≤ V_{DDIO} ≤ 2.7 V, I_{OL} = 2.5 mA	 — —		 0.5 0.5	 V V	1
V_{OL}	Output low voltage — High drive pad • 2.7 V ≤ V_{DDIO} ≤ 3.6 V, I_{OL} = 20 mA • 1.71 V ≤ V_{DDIO} ≤ 2.7 V, I_{OL} = 10 mA	 — —		 0.5 0.5	 V V	1
I_{OLT}	Output low current total for all ports	—		100	mA	
I_{IN}	Input leakage current (per pin) for full temperature range	—		1	µA	2
I_{IN}	Input leakage current (per pin) at 25 °C	—		0.025	µA	2
I_{IN}	Input leakage current (total all pins) for full temperature range	—		41	µA	2
I_{OZ}	Hi-Z (off-state) leakage current (per pin)	—		1	µA	
R_{PU}	Internal pullup resistors	20		50	kΩ	3

1. PTC[12:7], PTD[11:8], and PTE[11:10] I/O have both high drive and normal drive capability selected by the associated PORTx_PCRn[DSE] control bit. All other GPIOs are normal drive only. PTD[7:2], PTE[12,9:8,5:1], PTB[2,0] are also fast pins.
2. Measured at V_{DDIO} = 3.6 V
3. Measured at V_{DDIO} supply voltage = V_{DDIO} min and Vinput = V_{SS}

4.3.2.4 Power mode transition operating behaviors

All specifications in the following table assume this clock configuration with only CPU0 in Run mode and CPU1 disabled:

- CPU and system clocks = 48 MHz
- Bus and flash clock = 24 MHz
- SCG configured in FIRC mode; peripheral functional clocks from FIRCDIV3_CLK and USB clock from FIRCDIV1_CLK

Table 68. Power mode transition operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
t_{POR}	After a POR event, amount of time from the point V_{DDIO1} reaches 1.71 V and V_{DD_CORE} reaches 1.14 V to execution of the first instruction across the operating temperature range of the chip.	—	—	TBD	µs	1

Table continues on the next page...

Table 68. Power mode transition operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	• VLLS0/VLLS1 → RUN	—	272	353.6	µs	
	• VLLS2/VLLS3 → RUN	—	13.1	17.0	µs	
	• LLS → RUN	—	7.2	9.4	µs	
	• VLPS → RUN	—	3.5	4.6	µs	
	• STOP → RUN	—	3.5	4.6	µs	

1. Normal boot (FTFE_FOPT[BOOT_MODE]=1 and FTFE_FOPT[BOOT_CLK]=1).

4.3.2.5 Power consumption operating behaviors

4.3.2.5.1 Power consumption operating behaviors in regulator mode

The current parameters in the table below are derived from

- code executing a while(1) loop from flash, unless otherwise noted
- Core and system clocks running at 48 MHz, bus and flash clocks running at 24 MHz
- LPFLL at 48 MHz
- VDD_DCDC connected to VDDIO1 and VDDIO2

Symbol	Description	Temp (°C)	Active core	LDO (VDD_DCDC=3V)			DCDC (VDD_DCDC=3.3V)			Unit	Notes
				Min.	Typ.	Max	Min.	Typ.	Max		
I_{DD_DCDC}	Active core in RUN Inactive core in STOP while (1) loop All peripheral clocks disabled Execution from flash	25	0	TBD	5.8651189	6.4516308	TBD	3.4923734	3.8416107	mA	
			1	TBD	3.4103725	3.7514097	TBD	2.5025308	2.7527839		
			0 & 1	TBD	7.3966747	8.1363422	TBD	4.1223253	4.5345578		
		70	0	TBD	6.0877483	6.6965232	TBD	3.6289759	3.9918735		
			1	TBD	3.5917656	3.9509422	TBD	2.6190926	2.8810019		
			0 & 1	TBD	7.6752774	8.4428051	TBD	4.2888951	4.7177846		
		85	0	TBD	6.4058396	7.0464236	TBD	3.7855284	4.1640813		

Table continues on the next page...

Symbol	Description	Temp (°C)	Active core	LDO (VDD_DCDC=3V)			DCDC (VDD_DCDC=3.3V)			Unit	Notes
				Min.	Typ.	Max	Min.	Typ.	Max		
			1	TBD	3.8134 753	4.1948 228	TBD	2.7356 746	3.0092 421		
			0 & 1	TBD	8.0692 371	8.8761 608	TBD	4.4754 444	4.9229 888		
		105	0	TBD	7.0855 275	7.7940 803	TBD	3.0683 430	4.6124 974		
			1	TBD	4.3426 780	4.7769 458	TBD	3.0683 430	3.3751 773		
			0 & 1	TBD	8.8990 440	9.7889 484	TBD	4.9480 220	5.4428 242		
I_{DD_DCDC}	Active core in RUN Inactive core in STOP while (1) loop All peripheral clocks enabled Execution from flash	25	0	TBD	7.5362 928	8.2899 221	TBD	4.1772 545	4.5949 799	mA	
			1	TBD	4.7673 294	5.2440 623	TBD	3.0424 242	3.3466 667		
			0 & 1	TBD	10.275 0732	11.302 5805	TBD	5.3221 247	5.8543 372		
		70	0	TBD	7.7700 343	8.5470 377	TBD	4.3238 144	4.7561 959		
			1	TBD	4.9546 981	5.4501 679	TBD	3.1690 031	3.4859 035		
			0 & 1	TBD	10.579 1583	11.637 0742	TBD	5.5187 131	6.0705 844		
		85	0	TBD	8.0940 891	8.9034 980	TBD	4.4803 242	4.9283 566		
			1	TBD	5.2020 246	5.7222 271	TBD	3.5269 206	3.8796 126		
			0 & 1	TBD	10.991 0137	12.090 1150	TBD	5.7153 530	6.2868 883		
		105	0	TBD	8.7841 295	9.6625 425	TBD	4.9028 845	5.3931 730		
			1	TBD	5.7615 805	6.3377 386	TBD	3.6430 910	4.0074 001		
			0 & 1	TBD	11.881 4250	13.069 5675	TBD	6.2227 525	6.8450 278		
I_{DD_DCDC}	Active core in RUN Inactive core in STOP while (1) loop Compute Operation Execution from flash	25	0	TBD	5.2461 688	5.7707 856	TBD	3.1994 735	3.5194 208	mA	
			1	TBD	2.8215 352	3.1036 887	TBD	2.2296 502	2.4526 152		
			0 & 1	TBD	6.6631 669	7.3294 836	TBD	3.7794 404	4.1573 844		
		70	0	TBD	5.4587 041	6.0045 745	TBD	3.3354 144	3.6689 559		
			1	TBD	2.9876 701	3.2864 371	TBD	2.3355 965	2.5691 561		

Table continues on the next page...

Symbol	Description	Temp (°C)	Active core	LDO (VDD_DCDC=3V)			DCDC (VDD_DCDC=3.3V)			Unit	Notes
				Min.	Typ.	Max	Min.	Typ.	Max		
			0 & 1	TBD	6.9413 711	7.6355 082	TBD	3.9403 972	4.3344 369		
		85	0	TBD	5.7763 939	6.3540 332	TBD	3.4868 325	3.8355 158		
			1	TBD	3.2189 408	3.5408 349	TBD	2.4519 518	2.6971 470		
			0 & 1	TBD	7.3298 974	8.0628 872	TBD	4.1216 783	4.5338 461		
		105	0	TBD	6.4509 165	7.0960 082	TBD	3.8840 025	4.2724 028		
			1	TBD	3.7432 095	4.1175 305	TBD	2.7842 020	3.0626 222		
			0 & 1	TBD	8.1595 655	8.9755 221	TBD	4.5940 790	5.0534 869		
I_{DD_DCDC}	Active core in RUN Inactive core in STOP Coremark benchmark code Compute Operation Execution from flash	25	0	TBD	5.3445 974	5.8790 572	TBD	3.4994 804	3.8494 285	mA	
			1	TBD	4.7275 289	5.2002 818	TBD	2.9995 346	3.2994 880		
			0 & 1	TBD	8.8717 311	9.7589 043	TBD	4.8743 648	5.3618 013		
		70	0	TBD	5.5775 821	6.1353 403	TBD	3.6304 379	3.9934 817		
			1	TBD	4.8148 045	5.2962 849	TBD	3.1104 418	3.4214 859		
			0 & 1	TBD	8.9860 364	9.8846 400	TBD	5.0502 785	5.5553 063		
		85	0	TBD	6.2106 812	6.8317 494	TBD	3.7417 492	4.1159 241		
			1	TBD	5.0620 747	5.5682 821	TBD	3.1067 417	3.4174 159		
			0 & 1	TBD	9.5418 466	10.496 0313	TBD	5.0616 131	5.5677 745		
		105	0	TBD	6.7106 085	7.3816 694	TBD	4.1190 060	4.5309 066		
			1	TBD	5.6565 470	6.2222 017	TBD	3.4441 385	3.7885 524		
			0 & 1	TBD	10.212 4725	11.233 7198	TBD	5.6539 440	6.2193 384		
I_{DD_DCDC}	Active core in high speed RUN Inactive core in STOP while (1) loop. All peripheral clocks disabled. Execution	25	0	TBD	10.218 0003	11.239 8003	TBD	5.9754 302	6.5729 732	mA	
			1	TBD	5.3382 864	5.8721 150	TBD	3.5623 238	3.9185 562		
			0 & 1	TBD	12.814 2366	14.095 6603	TBD	7.2100 589	7.9310 648		

Table continues on the next page...

Symbol	Description	Temp (°C)	Active core	LDO (VDD_DCDC=3V)			DCDC (VDD_DCDC=3.3V)			Unit	Notes
				Min.	Typ.	Max	Min.	Typ.	Max		
	from flash Core V_{DD} = 1.4 V. Core clock = 72 MHz	70	0	TBD	10.563 4165	11.619 7582	TBD	6.1833 922	6.8017 314		
			1	TBD	5.6602 312	6.2262 544	TBD	3.7318 548	4.1050 403		
			0 & 1	TBD	13.198 5246	14.518 3771	TBD	7.4382 517	8.1820 768		
		85	0	TBD	11.073 3583	12.180 6941	TBD	6.4253 266	7.0678 592		
			1	TBD	6.1177 700	6.7295 470	TBD	3.9474 052	4.3421 457		
			0 & 1	TBD	13.691 0560	15.060 1616	TBD	7.6852 232	8.4537 455		
		105	0	TBD	12.068 4150	13.275 2565	TBD	7.0534 300	7.7587 730		
			1	TBD	7.0870 300	7.7957 330	TBD	4.5342 500	4.9876 750		
			0 & 1	TBD	14.687 1450	16.155 8595	TBD	8.3381 700	9.1719 870		
I_{DD_DCDC}	Active core in high speed RUN Inactive core in STOP while (1) loop All peripheral clocks enabled Execution from flash Core Vdd = 1.4V Core clock = 72MHz	25	0	TBD	12.819 1801	14.101 0981	TBD	7.2150 338	7.9365 372	mA	
			1	TBD	7.4387 438	8.1826 182	TBD	4.5122 387	4.9634 626		
			0 & 1	TBD	17.300 8086	19.030 8894	TBD	9.4198 050	10.361 7855		
		70	0	TBD	13.213 6074	14.534 9682	TBD	7.4483 007	8.1931 308		
			1	TBD	7.7917 474	8.5709 222	TBD	4.7115 303	5.1826 834		
			0 & 1	TBD	17.755 0556	19.530 5612	TBD	9.7030 572	10.673 3630		
		85	0	TBD	13.735 8550	15.109 4405	TBD	7.7051 844	8.4757 028		
			1	TBD	8.2703 248	9.0973 573	TBD	4.9322 609	5.4254 870		
			0 & 1	TBD	18.248 5860	20.073 4446	TBD	9.9748 488	10.972 3337		
		105	0	TBD	14.777 1950	16.254 9145	TBD	8.3732 700	9.2105 970		
			1	TBD	9.2851 450	10.213 6595	TBD	5.5539 900	6.1093 890		
			0 & 1	TBD	19.330 7100	21.263 7810	TBD	10.688 0250	11.756 8275		

Table continues on the next page...

Symbol	Description	Temp (°C)	Active core	LDO (VDD_DCDC=3V)			DCDC (VDD_DCDC=3.3V)			Unit	Notes
				Min.	Typ.	Max	Min.	Typ.	Max		
I_{DD_DCDC}	Active core in high speed RUN Inactive core in STOP, Compute Operation Execution from flash Core Vdd = 1.4V Core clock = 72MHz	25	0	TBD	9.4742955	10.4217251	TBD	5.5924751	6.1517226	mA	
			1	TBD	4.6345561	5.0980117	TBD	3.2045045	3.5249549		
			0 & 1	TBD	11.9349895	13.1284885	TBD	6.7524689	7.4277158		
		70	0	TBD	9.8293219	10.8122541	TBD	5.7949851	6.3744836		
			1	TBD	4.9663010	5.4629311	TBD	3.3733394	3.7106734		
			0 & 1	TBD	12.3146500	13.5461150	TBD	6.9798909	7.6778800		
		85	0	TBD	10.3185410	11.3503951	TBD	6.0316590	6.6348249		
			1	TBD	5.3935126	5.9328639	TBD	3.5837069	3.9420776		
			0 & 1	TBD	12.8067876	14.0874663	TBD	7.2264905	7.9491396		
		105	0	TBD	11.3088900	12.4397790	TBD	6.6545900	7.3200490		
			1	TBD	6.3626300	6.9988930	TBD	4.1653900	4.5819290		
			0 & 1	TBD	13.8125450	15.1937995	TBD	7.8593650	8.6453015		
I_{DD_DCDC}	Active core in high speed RUN Inactive core in STOP Coremark benchmark code; Execution from flash Core Vdd = 1.4V Core clock = 72MHz	25	0	TBD	10.2316640	11.2548304	TBD	5.9625644	6.5588208	mA	
			1	TBD	8.0329883	8.8362871	TBD	4.6992878	5.1692166		
			0 & 1	TBD	15.7513001	17.3264301	TBD	8.6471733	9.5118907		
		70	0	TBD	10.3473410	11.3820751	TBD	6.2650069	6.8915076		
			1	TBD	7.8810412	8.8362871	TBD	4.6832397	5.1515636		
			0 & 1	TBD	16.0362923	17.6399215	TBD	9.0048652	9.9053517		
		85	0	TBD	10.8776352	11.9653987	TBD	6.3516303	6.9867933		
			1	TBD	8.3945135	9.2339649	TBD	5.0736881	5.5810569		
			0 & 1	TBD	16.7142115	18.3856327	TBD	8.9365333	9.8301866		
		105	0	TBD	12.1231800	13.3354980	TBD	6.9794450	7.6773895		

Table continues on the next page...

Symbol	Description	Temp (°C)	Active core	LDO (VDD_DCDC=3V)			DCDC (VDD_DCDC=3.3V)			Unit	Notes
				Min.	Typ.	Max	Min.	Typ.	Max		
			1	TBD	9.7353 200	10.708 8520	TBD	5.5524 900	6.1077 390		
			0 & 1	TBD	17.830 9150	19.614 0065	TBD	9.8116 850	10.792 8535		
I_{DD_DCDC}	Active core in WAIT Inactive core in STOP All peripheral clocks disabled	25	0	TBD	2.7318 225	3.0050 048	TBD	0.5042 153	0.5546 368	mA	
			1	TBD	2.3875 208	2.6262 729	TBD	0.8014 842	0.8816 326		
			0 & 1	TBD	3.2308 192	3.5539 011	TBD	2.2375 536	2.4613 089		
		70	0	TBD	2.9377 668	3.2315 435	TBD	0.5405 379	0.5945 917		
			1	TBD	2.5534 335	2.8087 769	TBD	0.8454 344	0.9299 779		
			0 & 1	TBD	3.4868 897	3.8355 787	TBD	2.3592 414	2.5951 655		
		85	0	TBD	3.2339 529	3.5573 481	TBD	TBD	TBD		
			1	TBD	2.7844 934	3.0629 427	TBD	TBD	TBD		
			0 & 1	TBD	3.8534 339	4.2387 772	TBD	2.5056 867	2.7562 554		
		105	0	TBD	3.9031 480	4.3324 943	TBD	TBD	TBD		
			1	TBD	3.7397 096	3.6668 684	TBD	TBD	TBD		
			0 & 1	TBD	4.6723 855	5.1863 479	TBD	2.8933 210	3.2115 863		
I_{DD_DCDC}	Active core in WAIT Inactive core in STOP All peripheral clocks disabled Flash disabled	25	0	TBD	4.3982 298	4.8380 528	TBD	2.1026 105	2.3128 715	mA	
			1	TBD	3.7397 096	4.1136 806	TBD	2.4326 011	2.6758 612		
			0 & 1	TBD	6.0996 947	6.7096 642	TBD	2.9024 704	3.1927 175		
		70	0	TBD	4.6100 992	5.0711 092	TBD	2.2142 536	2.4356 790		
			1	TBD	3.9211 695	4.3132 865	TBD	2.5792 107	2.8371 317		
			0 & 1	TBD	6.3824 161	7.0206 578	TBD	3.0340 810	3.3374 891		
		85	0	TBD	4.9172 868	5.4090 155	TBD	2.3257 038	2.5582 742		
			1	TBD	4.1681 535	4.5849 689	TBD	2.7456 277	3.0201 905		

Table continues on the next page...

Symbol	Description	Temp (°C)	Active core	LDO (VDD_DCDC=3V)			DCDC (VDD_DCDC=3.3V)			Unit	Notes
				Min.	Typ.	Max	Min.	Typ.	Max		
			0 & 1	TBD	6.7704 384	7.4474 823	TBD	3.1755 614	3.4931 175		
		105	0	TBD	5.5867 315	6.2012 720	TBD	2.6534 595	2.9453 400		
			1	TBD	4.7224 495	5.2419 189	TBD	3.2033 400	3.5557 074		
			0 & 1	TBD	7.6251 305	8.4638 949	TBD	3.5784 120	3.9720 373		
I_{DD_DCDC}	Both cores in PSTOP2 Flash disabled	25	--	TBD	1.4686 224	2.4232 270	--	--	--	mA	
		70	--	TBD	1.7237 184	2.8786 097	--	--	--		
		85	--	TBD	2.1095 349	3.4807 326	--	--	--		
		105	--	TBD	2.9682 465	4.7788 769	--	--	--		
I_{DD_DCDC}	Active core in VLPR Inactive core in VLPS while (1) loop All peripheral clocks disabled Execution from flash Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz	25	0	TBD	0.8125 956	0.8938 551	--	0.9236 022	--	mA	
			1	TBD	0.4484 704	0.4933 175	--	0.4537 492	--		
			0 & 1	TBD	1.0165 950	1.1182 545	--	1.1307 699	--		
		70	0	TBD	0.8703 438	0.9573 781	--	--	--		
			1	TBD	0.4980 829	0.5478 912	--	--	--		
			0 & 1	TBD	1.0764 042	1.1840 446	--	--	--		
		85	0	TBD	0.9414 290	1.0355 719	--	--	--		
			1	TBD	0.5704 961	0.6275 457	--	--	--		
			0 & 1	TBD	1.1488 764	1.2637 641	--	--	--		
		105	0	TBD	1.1129 920	1.2242 912	--	--	--		
			1	TBD	0.7409 135	0.8150 049	--	--	--		
			0 & 1	TBD	1.3242 965	1.4567 262	--	--	--		
I_{DD_DCDC}	Active core in VLPR Inactive core in VLPS while (1) loop All peripheral clocks	25	0	TBD	1.0390 560	1.1429 616	--	--	--	mA	
			1	TBD	0.6384 310	0.9959 524	--	--	--		

Table continues on the next page...

Symbol	Description	Temp (°C)	Active core	LDO (VDD_DCDC=3V)			DCDC (VDD_DCDC=3.3V)			Unit	Notes
				Min.	Typ.	Max	Min.	Typ.	Max		
	enabled Execution from flash Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz		0 & 1	TBD	1.4058 049	1.5463 854	--	--	--		
		70	0	TBD	1.0966 464	1.2063 111	--	--	--		
			1	TBD	0.6903 102	1.1321 088	--	--	--		
			0 & 1	TBD	1.4668 090	1.6134 899	--	--	--		
		85	0	TBD	1.1736 655	1.2910 320	--	--	--		
			1	TBD	0.7631 074	1.2438 650	--	--	--		
			0 & 1	TBD	1.5385 910	1.6924 501	--	--	--		
		105	0	TBD	1.3441 615	1.4785 777	--	--	--		
			1	TBD	0.9320 920	1.4820 263	--	--	--		
			0 & 1	TBD	1.7143 135	1.8857 449	--	--	--		
I_{DD_DCDC}	Active core in VLPR Inactive core in VLPS while (1) loop Compute Operation Execution from flash Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz	25	0	TBD	0.7851 406	0.8636 547	--	--	--	mA	
			1	TBD	0.4252 546	0.6633 972	--	--	--		
			0 & 1	TBD	0.9876 227	1.0863 850	--	--	--		
		70	0	TBD	0.8375 459	0.9213 005	--	--	--		
			1	TBD	0.4732 995	0.7762 113	--	--	--		
			0 & 1	TBD	1.0481 555	1.1529 710	--	--	--		
		85	0	TBD	0.9160 067	1.0076 074	--	--	--		
			1	TBD	0.5432 823	0.8855 502	--	--	--		
			0 & 1	TBD	1.1238 677	1.2362 544	--	--	--		
		105	0	TBD	1.0839 955	1.1923 951	--	--	--		
			1	TBD	0.7113 835	1.1310 998	--	--	--		
			0 & 1	TBD	1.2940 520	1.4234 572	--	--	--		

Table continues on the next page...

Symbol	Description	Temp (°C)	Active core	LDO (VDD_DCDC=3V)			DCDC (VDD_DCDC=3.3V)			Unit	Notes
				Min.	Typ.	Max	Min.	Typ.	Max		
I_{DD_DCDC}	Active core in VLPR Inactive core in VLPS Coremark benchmark code Compute Operation Execution from flash Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz	25	0	TBD	0.8983 307	0.9881 638	--	--	--	mA	
			1	TBD	0.7530 949	1.1748 280	--	--	--		
			0 & 1	TBD	1.3206 901	1.4527 591	--	--	--		
		70	0	TBD	0.9003 378	0.9903 716	--	--	--		
			1	TBD	0.7505 096	1.2308 358	--	--	--		
			0 & 1	TBD	1.4567 849	1.6024 633	--	--	--		
		85	0	TBD	0.9764 007	1.0740 407	--	--	--		
			1	TBD	0.8481 384	1.3824 656	--	--	--		
			0 & 1	TBD	1.5686 854	1.7255 540	--	--	--		
		105	0	TBD	1.1542 810	1.2697 091	--	--	--		
			1	TBD	1.0542 210	1.6762 114	--	--	--		
			0 & 1	TBD	1.7041 740	1.8745 914	--	--	--		
I_{DD_DCDC}	Active core in VLPW Inactive core in VLPS All peripheral clocks disabled Flash disabled Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz	25	0	TBD	0.3491 953	0.3841 148	--	--	--	mA	
			1	TBD	0.3057 422	0.4769 578	--	--	--		
			0 & 1	TBD	0.4113 682	0.4525 051	--	--	--		
		70	0	TBD	0.3972 241	0.4369 465	--	--	--		
			1	TBD	0.3536 407	0.5799 708	--	--	--		
			0 & 1	TBD	0.4560 503	0.5016 554	--	--	--		
		85	0	TBD	0.4701 034	0.5171 138	--	--	--		
			1	TBD	0.4243 183	0.6916 388	--	--	--		
			0 & 1	TBD	0.5303 140	0.5833 454	--	--	--		
		105	0	TBD	0.6366 055	0.7320 963	--	--	--		

Table continues on the next page...

Symbol	Description	Temp (°C)	Active core	LDO (VDD_DCDC=3V)			DCDC (VDD_DCDC=3.3V)			Unit	Notes
				Min.	Typ.	Max	Min.	Typ.	Max		
			1	TBD	0.5927040	0.9423994	--	--	--		
			0 & 1	TBD	0.7035510	0.8090836	--	--	--		

4.3.2.5.2 Power consumption operating behaviors in bypass mode

The current parameters in the table below are derived from

- code executing a while(1)
- loop from flash, unless otherwise noted
- Core and system clocks running at 48 MHz, bus and flash clocks running at 24 MHz
- LPFLL at 48MHz

Symbol	Description	Temp (°C)	Active core	Core		VDDIO1		VDDIO2		Unit	Notes
				Typ.	Max	Typ.	Max	Typ.	Max		
I_{DD}	Active core in RUN Inactive core in STOP while (1) loop All peripheral clocks disabled Execution from flash	25	0	5.060000	5.566000	0.194135	0.2135485	0.0000161	0.0000177	mA	
			1	2.860000	3.146000	0.194160	0.2135760	0.0000148	0.0000163		
			0 & 1	6.365000	7.001500	0.194115	0.2135265	0.0000162	0.0000179		
		70	0	5.275000	5.802500	0.200390	0.2204290	0.0002092	0.0002302		
			1	3.020000	3.322000	0.200290	0.2203190	0.0002101	0.0002311		
			0 & 1	6.605000	7.265500	0.200365	0.2204015	0.0002093	0.0002303		
		85	0	5.460000	6.006000	0.204280	0.2247080	0.0004763	0.0005239		
			1	3.205000	3.525500	0.204325	0.2247575	0.0004741	0.0005215		
			0 & 1	6.870000	7.557000	0.204210	0.2246310	0.0004762	0.0005238		
		105	0	5.970000	6.567000	0.214045	0.2354495	0.0013750	0.0015125		
			1	3.620000	3.982000	0.214100	0.2355100	0.0013700	0.0015070		
			0 & 1	7.475000	8.222500	0.213920	0.2353120	0.0013700	0.0015070		

Table continues on the next page...

Symbol	Description	Temp (°C)	Active core	Core		VDDIO1		VDDIO2		Unit	Notes
				Typ.	Max	Typ.	Max	Typ.	Max		
I_{DD}	Active core in RUN Inactive core in STOP while (1) loop All peripheral clocks enabled Execution from flash	25	0	6.485000	7.1335000	0.194125	0.2135375	0.0000153	0.0000168	mA	
			1	4.090000	4.4990000	0.194135	0.2135485	0.0000151	0.0000166		
			0 & 1	8.685000	9.5535000	0.194056	0.2134605	0.0000154	0.0000170		
		70	0	6.665000	7.3315000	0.200390	0.2204290	0.0002100	0.0002311		
			1	4.260000	4.6860000	0.200390	0.2204190	0.0002091	0.0002300		
			0 & 1	8.915000	9.8065000	0.200310	0.2203410	0.0002101	0.0002311		
		85	0	6.885000	7.5735000	0.204195	0.2246145	0.0004738	0.0005211		
			1	4.430000	4.8730000	0.204305	0.2247355	0.0004725	0.0005198		
			0 & 1	9.180000	10.0980000	0.204125	0.2245375	0.0004727	0.0005200		
		105	0	7.355000	8.0905000	0.213935	0.2353285	0.0013700	0.0015070		
			1	4.870000	5.3570000	0.214115	0.2355265	0.0013700	0.0015070		
			0 & 1	9.755000	10.7305000	0.213975	0.2353725	0.0013750	0.0015125		
I_{DD}	Active core in RUN Inactive core in STOP while (1) loop Compute Operation Execution from flash	25	0	4.570000	5.0270000	0.138110	0.1519210	0.0000151	0.0000166	mA	
			1	2.360000	2.5960000	0.138160	0.1519760	0.0000151	0.0000166		
			0 & 1	5.795000	6.3745000	0.138060	0.1518660	0.0000169	0.0000186		
		70	0	4.770000	5.2470000	0.143660	0.1580260	0.0002110	0.0002321		
			1	2.525000	2.7775000	0.143725	0.1580975	0.0002104	0.0002314		
			0 & 1	6.035000	6.6385000	0.143620	0.1579820	0.0002094	0.0002304		
		85	0	4.965000	5.4615000	0.147345	0.1620795	0.0004724	0.0005196		
			1	2.700000	2.9700000	0.147425	0.1621675	0.0004710	0.0005181		
			0 & 1	6.290000	6.9190000	0.147330	0.1620630	0.0004714	0.0005186		
		105	0	5.495000	6.0445000	0.156855	0.1725405	0.0013650	0.0015015		

Table continues on the next page...

Symbol	Description	Temp (°C)	Active core	Core		VDDIO1		VDDIO2		Unit	Notes
				Typ.	Max	Typ.	Max	Typ.	Max		
			1	3.130000	3.443000	0.156915	0.172606 5	0.0013700	0.0015070		
			0 & 1	6.910000	7.601000	0.156840	0.172606 5	0.0013750	0.0015125		
I_{DD}	Active core in RUN Inactive core in STOP Coremark benchmark code Compute Operation Execution from flash	25	0	5.210000	5.731000	0.138095	0.151904 5	0.0000155	0.0000171	mA	
			1	3.820000	4.202000	0.138125	0.151937 5	0.0000145	0.0000160		
			0 & 1	8.330000	9.163000	0.138000	0.151800 0	0.0000142	0.0000156		
		70	0	5.645000	6.209500 0	0.143670	0.158037 0	0.0002104	0.0002315		
			1	4.000000	4.400000	0.143685	0.158053 5	0.0002103	0.0002314		
			0 & 1	8.730000	9.603000	0.143570	0.157927 0	0.0002083	0.0002292		
		85	0	5.810000	6.391000	0.147345	0.162079 5	0.0004701	0.0005171		
			1	4.080000	4.488000	0.147370	0.162107 0	0.0004703	0.0005174		
			0 & 1	9.095000	10.004 5000	0.147265	0.161991 5	0.0004716	0.0005188		
		105	0	6.450000	7.095000	0.156890	0.172579 0	0.0013750	0.0015125		
			1	4.620000	5.082000	0.156885	0.172573 5	0.0013700	0.0015070		
			0 & 1	9.710000	10.681 0000	0.156845	0.172573 5	0.0013800	0.0015180		
I_{DD}	Active core in high speed RUN Inactive core in STOP while (1) loop All peripheral clocks disabled Execution from flash Core Vdd = 1.4V Core clock = 72MHz	25	0	9.205000	10.125 5000	0.533670	0.587037 0	0.0000155	0.0000170	mA	
			1	4.815000	5.296500 0	0.200405	0.220445 5	0.0000148	0.0000163		
			0 & 1	11.660 000	12.826 0000	0.533585	0.586943 5	0.0000157	0.0000173		
		70	0	9.545000	10.499 5000	0.543745	0.598119 5	0.0002102	0.0002312		
			1	5.160000	5.676000	0.206865	0.227551 5	0.0002106	0.0002317		
			0 & 1	12.025 000	13.227 5000	0.543845	0.598229 5	0.0002110	0.0002321		
		85	0	9.880000	10.868 0000	0.548840	0.603724 0	0.0004703	0.0005173		
			1	5.515000	6.066500 0	0.210755	0.231830 5	0.0004679	0.0005147		

Table continues on the next page...

Symbol	Description	Temp (°C)	Active core	Core		VDDIO1		VDDIO2		Unit	Notes
				Typ.	Max	Typ.	Max	Typ.	Max		
			0 & 1	12.360 000	13.596 0000	0.5485 30	0.6033 830	0.0004 740	0.0005 214		
		105	0	10.720 000	11.792 0000	0.5600 05	0.6160 055	0.0013 350	0.0014 685		
			1	6.3550 00	6.9905 000	0.2207 10	0.2427 810	0.0013 250	0.0014 575		
			0 & 1	13.200 000	14.520 0000	0.5600 35	0.6160 385	0.0013 350	0.0014 685		
I_{DD}	Active core in high speed RUN Inactive core in STOP while (1) loop All peripheral clocks enabled Execution from flash Core Vdd = 1.4V Core clock = 72MHz	25	0	11.670 000	12.837 0000	0.5336 05	0.5869 655	0.0000 161	0.0000 178	mA	
			1	6.8500 00	7.5350 000	0.2004 45	0.2204 895	0.0000 154	0.0000 169		
			0 & 1	15.885 000	17.473 5000	0.5335 45	0.5868 995	0.0000 159	0.0000 175		
		70	0	12.040 000	13.244 0000	0.5438 30	0.5982 130	0.0002 118	0.0002 329		
			1	7.2100 00	7.9310 000	0.2065 85	0.2272 435	0.0002 112	0.0002 323		
			0 & 1	16.255 000	17.880 5000	0.5437 00	0.5980 700	0.0002 117	0.0002 329		
		85	0	12.385 000	13.623 5000	0.5485 55	0.6034 105	0.0004 699	0.0005 169		
			1	7.5800 00	8.3380 000	0.2105 25	0.2315 775	0.0004 724	0.0005 197		
			0 & 1	16.615 000	18.276 5000	0.5485 55	0.6034 105	0.0004 716	0.0005 188		
		105	0	13.250 000	14.575 0000	0.5598 65	0.6158 515	0.0013 350	0.0014 685		
			1	8.4600 00	9.3060 000	0.2207 50	0.2428 250	0.0013 350	0.0014 685		
			0 & 1	17.495 000	19.244 5000	0.5598 30	0.6158 130	0.0013 450	0.0014 795		
I_{DD}	Active core in high speed RUN Inactive core in STOP while (1) loop Compute Operation Execution from flash Core Vdd = 1.4V Core clock = 72MHz	25	0	8.5450 00	9.3995 000	0.4777 10	0.5254 810	0.0000 150	0.0000 165	mA	
			1	4.1800 00	4.5980 000	0.1446 45	0.1591 095	0.0000 155	0.0000 171		
			0 & 1	10.885 000	11.973 5000	0.4777 80	0.5255 580	0.0000 162	0.0000 178		
		70	0	8.8850 00	9.7735 000	0.4874 95	0.5362 445	0.0002 094	0.0002 304		
			1	4.5250 00	4.9775 000	0.1503 15	0.1653 465	0.0002 096	0.0002 315		
			0 & 1	11.245 000	12.369 5000	0.4875 10	0.5362 610	0.0002 111	0.0002 322		

Table continues on the next page...

Symbol	Description	Temp (°C)	Active core	Core		VDDIO1		VDDIO2		Unit	Notes
				Typ.	Max	Typ.	Max	Typ.	Max		
		85	0	9.220000	10.1420000	0.492135	0.5413485	0.0004694	0.0005163		
			1	4.880000	5.3680000	0.153930	0.1693230	0.0004668	0.0005135		
			0 & 1	11.585000	12.7435000	0.491985	0.5411835	0.0004697	0.0005167		
		105	0	10.080000	11.0880000	0.502915	0.5532065	0.0013350	0.0014685		
			1	5.725000	6.2975000	0.163740	0.1801140	0.0013400	0.0014740		
			0 & 1	12.450000	13.6950000	0.502925	0.5532175	0.0013400	0.0014740		
I_{DD}	Active core in high speed RUN Inactive core in STOP Coremark benchmark code Compute Operation Execution from flash Core Vdd = 1.4V Core clock = 72MHz	25	0	9.725000	10.6975000	0.477850	0.5256350	0.0000153	0.0000168	mA	
			1	6.955000	7.6505000	0.144415	0.1588565	0.0000156	0.0000171		
			0 & 1	14.710000	16.1810000	0.477615	0.5253765	0.0000167	0.0000183		
		70	0	9.235000	10.1585000	0.487495	0.5362445	0.0002099	0.0002309		
			1	7.840000	8.6240000	0.150215	0.1652365	0.0002101	0.0002311		
			0 & 1	15.015000	16.5165000	0.487315	0.5360465	0.0002135	0.0002349		
		85	0	9.375000	10.3125000	0.492040	0.5412440	0.0004692	0.0005161		
			1	7.690000	8.4590000	0.153945	0.1693395	0.0004663	0.0005129		
			0 & 1	15.305000	16.8355000	0.492040	0.5412440	0.0004736	0.0005209		
		105	0	11.035000	12.1385000	0.502965	0.5532615	0.0013450	0.0014795		
			1	9.015000	9.9165000	0.163580	0.1799380	0.0013350	0.0014685		
			0 & 1	15.620000	17.1820000	0.502825	0.5531075	0.0013450	0.0014795		
I_{DD}	Active core in WAIT Inactive core in STOP All peripheral clocks disabled	25	0	2.225000	2.4475000	0.194160	0.2135760	0.0000152	0.0000167	mA	
			1	1.900000	2.0900000	0.194190	0.2136090	0.0000149	0.0000164		
			0 & 1	2.680000	2.9480000	0.194115	0.2135265	0.0000163	0.0000179		
		70	0	2.435000	2.6785000	0.200400	0.2204400	0.0002083	0.0002291		

Table continues on the next page...

Symbol	Description	Temp (°C)	Active core	Core		VDDIO1		VDDIO2		Unit	Notes
				Typ.	Max	Typ.	Max	Typ.	Max		
			1	2.060000	2.266000	0.200335	0.2203685	0.0002065	0.0002272		
			0 & 1	2.935000	3.228500	0.200270	0.2202970	0.0002088	0.0002297		
		85	0	2.645000	2.909500	0.204350	0.2247850	0.0004666	0.0005132		
			1	2.225000	2.447500	0.204305	0.2247355	0.0004664	0.0005131		
			0 & 1	3.200000	3.520000	0.204290	0.2247190	0.0004646	0.0005111		
		105	0	3.190000	3.540900	0.214045	0.2375900	0.0013650	0.0015152		
			1	2.665000	2.958150	0.214210	0.2377731	0.0013700	0.0015207		
			0 & 1	3.880000	4.306800	0.214075	0.2376232	0.0013700	0.0015207		
I_{DD}	Active core in WAIT Inactive core in STOP All peripheral clocks disabled Flash disabled	25	0	3.755000	4.130500	0.194145	0.2135595	0.0000149	0.0000164	mA	
			1	3.155000	3.470500	0.194170	0.2135430	0.0000158	0.0000173		
			0 & 1	5.245000	5.769500	0.194130	0.2135430	0.0000158	0.0000173		
		70	0	3.955000	4.350500	0.200360	0.2203960	0.0002086	0.0002294		
			1	3.320000	3.652000	0.200390	0.2204290	0.0002097	0.0002306		
			0 & 1	5.500000	6.050000	0.200360	0.2203960	0.0002097	0.0002307		
		85	0	4.155000	4.570500	0.204320	0.2247520	0.0004651	0.0005116		
			1	3.500000	3.850000	0.204330	0.2247630	0.0004678	0.0005146		
			0 & 1	5.745000	6.319500	0.204260	0.2246860	0.0004675	0.0005142		
		105	0	4.690000	5.205900	0.214065	0.2376122	0.0013650	0.0015152		
			1	3.940000	4.373400	0.214090	0.2376399	0.0013700	0.0015207		
			0 & 1	6.405000	7.109550	0.213930	0.2374623	0.0013700	0.0015207		
I_{DD}	Both cores in PSTOP2 Flash disabled	25	--	0.695445	1.147484	0.517925	0.8545762	0.0000153	0.0000252	mA	
		70	--	0.961155	1.605128	0.546755	0.9130808	0.0002080	0.0003473		

Table continues on the next page...

Symbol	Description	Temp (°C)	Active core	Core		VDDIO1		VDDIO2		Unit	Notes
				Typ.	Max	Typ.	Max	Typ.	Max		
		85	--	1.235000	2.037750	0.568310	0.937711	0.000465	0.000768		
		105	--	1.950000	3.139500	0.620830	0.999536	0.001370	0.002205		
I_{DD}	Active core in VLPR Inactive core in VLPS while (1) loop All peripheral clocks disabled Execution from flash Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz	25	0	0.765110	0.841621	0.056205	0.061825	0.000013	0.000014	mA	
			1	0.397390	0.437129	0.056215	0.061836	0.000014	0.000015		
			0 & 1	0.966850	1.063535	0.056205	0.061825	0.000014	0.000015		
		70	0	0.819845	0.901829	0.059695	0.065664	0.000208	0.000229		
			1	0.449135	0.494048	0.059725	0.065697	0.000207	0.000228		
			0 & 1	1.025205	1.127725	0.059700	0.065670	0.000207	0.000228		
		85	0	0.874085	0.961493	0.063040	0.069344	0.000470	0.000517		
			1	0.502720	0.552992	0.063040	0.069344	0.000468	0.000515		
			0 & 1	1.079730	1.187703	0.063065	0.069371	0.000467	0.000514		
		105	0	1.013885	1.115273	0.072620	0.079882	0.001360	0.001496		
			1	0.643700	0.708070	0.072675	0.079942	0.001360	0.001496		
			0 & 1	1.220000	1.342000	0.072650	0.079915	0.001360	0.001496		
I_{DD}	Active core in VLPR Inactive core in VLPS while (1) loop All peripheral clocks enabled Execution from flash Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz	25	0	0.990060	1.089066	0.056165	0.061781	0.000014	0.000015	mA	
			1	0.589900	0.920244	0.056150	0.087594	0.000015	0.000023		
			0 & 1	1.350000	1.485000	0.056165	0.061781	0.000015	0.000016		
		70	0	1.048785	1.153664	0.059740	0.065714	0.000207	0.000228		
			1	0.643400	1.055176	0.059735	0.097965	0.000208	0.000342		
			0 & 1	1.410000	1.551000	0.059705	0.065676	0.000209	0.000230		
		85	0	1.100000	1.210000	0.063025	0.069328	0.000466	0.000513		
			1	0.697190	1.136420	0.063015	0.102715	0.000463	0.000754		

Table continues on the next page...

Symbol	Description	Temp (°C)	Active core	Core		VDDIO1		VDDIO2		Unit	Notes
				Typ.	Max	Typ.	Max	Typ.	Max		
			0 & 1	1.465000	1.6115000	0.063005	0.0693055	0.0004646	0.0005110		
		105	0	1.245000	1.3695000	0.072630	0.0798930	0.0013600	0.0014960		
			1	0.836925	1.3307107	0.072650	0.1155135	0.0013600	0.0021624		
			0 & 1	1.605000	1.7655000	0.072740	0.0800140	0.0013650	0.0015015		
I_{DD}	Active core in VLPR Inactive core in VLPS while (1) loop Compute Operation Execution from flash Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz	25	0	0.739540	0.8134940	0.053905	0.0592955	0.0000151	0.0000166	mA	
			1	0.373860	0.5832216	0.053885	0.0840606	0.0000145	0.0000226		
			0 & 1	0.944090	1.0384990	0.053885	0.0592735	0.0000155	0.0000170		
		70	0	0.794235	0.8736585	0.057425	0.0631675	0.0002076	0.0002283		
			1	0.426990	0.7002636	0.057370	0.0940868	0.0002078	0.0003408		
			0 & 1	0.998370	1.0982070	0.057435	0.0631785	0.0002082	0.0002290		
		85	0	0.847725	0.9324975	0.060675	0.0667425	0.0004643	0.0005107		
			1	0.479830	0.7821229	0.060705	0.0989491	0.0004650	0.0007579		
			0 & 1	1.057165	1.1628815	0.060705	0.0667755	0.0004649	0.0005114		
		105	0	0.991295	1.0904245	0.070300	0.0773300	0.0013600	0.0014960		
			1	0.620610	0.9867699	0.070350	0.1118565	0.0013700	0.0021783		
			0 & 1	1.200000	1.3200000	0.070310	0.0773410	0.0013600	0.0014960		
I_{DD}	Active core in VLPR Inactive core in VLPS Coremark benchmark code Compute Operation Execution from flash Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz	25	0	0.832740	0.9160140	0.053905	0.0592955	0.0000145	0.0000160	mA	
			1	0.699710	1.0915476	0.053890	0.0840684	0.0000151	0.0000235		
			0 & 1	1.390000	1.5290000	0.053945	0.0593395	0.0000158	0.0000173		
		70	0	0.859770	0.9457470	0.057415	0.0631565	0.0002069	0.0002276		
			1	0.735630	1.2064332	0.057435	0.0941934	0.0002071	0.0003397		
			0 & 1	1.395000	1.5345000	0.057405	0.0631455	0.0002074	0.0002281		

Table continues on the next page...

Symbol	Description	Temp (°C)	Active core	Core		VDDIO1		VDDIO2		Unit	Notes
				Typ.	Max	Typ.	Max	Typ.	Max		
		85	0	0.907400	0.9981400	0.060705	0.0667755	0.0004666	0.0005133		
			1	0.773870	1.2614081	0.060715	0.0989654	0.0004675	0.0007621		
			0 & 1	1.450000	1.5950000	0.060725	0.0667975	0.0004643	0.0005107		
		105	0	1.100000	1.2100000	0.070335	0.0773685	0.0013600	0.0014960		
			1	0.982280	1.5618252	0.070405	0.1119439	0.0013650	0.0021704		
			0 & 1	1.670000	1.8370000	0.070355	0.0773905	0.0013650	0.0015015		
I_{DD}	Active core in VLPW Inactive core in VLPS All peripheral clocks disabled Flash disabled Slow IRC = 8 MHz Core = 8 MHz, bus = 4 MHz Flash = 1 MHz	25	0	0.298040	0.3278440	0.056195	0.0618145	0.0000149	0.0000164	mA	
			1	0.253375	0.3952650	0.056200	0.0876720	0.0000161	0.0000252		
			0 & 1	0.358580	0.3944380	0.056170	0.0617870	0.0000154	0.0000169		
		70	0	0.349290	0.3842190	0.059730	0.0657030	0.0002072	0.0002279		
			1	0.304110	0.4987404	0.059705	0.0979162	0.0002064	0.0003385		
			0 & 1	0.410020	0.4510220	0.059750	0.0657250	0.0002066	0.0002272		
		85	0	0.402000	0.4422000	0.063015	0.0693165	0.0004662	0.0005129		
			1	0.356640	0.5813232	0.062980	0.1026574	0.0004654	0.0007586		
			0 & 1	0.463080	0.5093880	0.063020	0.0693220	0.0004649	0.0005114		
		105	0	0.543985	0.6255827	0.072705	0.0836108	0.0013700	0.0015755		
			1	0.497370	0.7908183	0.072645	0.1155056	0.0013650	0.0021704		
			0 & 1	0.604360	0.6950140	0.072720	0.0836280	0.0013700	0.0015755		

4.3.2.5.3 Power consumption operating behaviors in low power mode

NOTE

Data for this table was collected in bypass mode except where otherwise noted.

Symbol	Description		Core		VDDIO1		VDDIO2		Unit	Notes
			Typ.	Max	Typ.	Max	Typ.	Max		
I_{DD_STOP}	Both cores are in STOP mode Core = 1.2V, VDDIO1 = VDDIO2 = 3V	25 °C	13.594	TBD	1.43	TBD	0.01532	TBD	µA	
		70 °C	164.44	TBD	5.21	TBD	0.33509	TBD		
		85 °C	352.76	TBD	11.16	TBD	0.87761	TBD		
		105 °C	821.67	TBD	30.00	TBD	2.65000	TBD		
I_{DD_VLPS}	Both cores are in Very Low Power STOP mode Core = 1.2V, VDDIO1 = VDDIO2 = 3V	25 °C	9.0509	TBD	1.50	TBD	0.01614	TBD	µA	
		70 °C	81.30	TBD	5.42	TBD	0.33092	TBD		
		85 °C	180.06	TBD	11.50	TBD	0.86987	TBD		
		105 °C	440.99	TBD	32.06	TBD	2.65000	TBD		
I_{DD_LLS}	Both cores are in Low Leakage STOP mode Core = 1.2V, VDDIO1 = VDDIO2 = 3V	25 °C	2.1166	TBD	1.58	TBD	0.01520	TBD	µA	
		70 °C	30.19	TBD	5.25	TBD	0.31557	TBD		
		85 °C	66.84	TBD	10.86	TBD	0.81976	TBD		
		105 °C	162.66	TBD	29.63	TBD	2.52000	TBD		
I_{DD_VLLS3}	Both cores are in VLLS3 mode; core = 1.2 V, VDDIO1 = VDDIO2 = 3 V[1]	25 °C	1.7105	TBD	1.32	TBD	0.01572	TBD	µA	
		70 °C	30.42	TBD	5.31	TBD	0.34199	TBD		
		85 °C	62.98	TBD	10.60	TBD	0.84299	TBD		
		105 °C	148.14	TBD	27.60	TBD	2.52000	TBD		
I_{DD_OFF}	Only the VBAT domain is powered with the RTC oscillator operating and all other supplies are at Vss.	25 °C	TBD	TBD	TBD	TBD	TBD	TBD	nA	
		70 °C	TBD	TBD	TBD	TBD	TBD	TBD		
		85 °C	TBD	TBD	TBD	TBD	TBD	TBD		
		105 °C	TBD	TBD	TBD	TBD	TBD	TBD		
I_{DD_VLLS1}	Both cores are in VLLS1 mode Core = 1.2V, VDDIO1 = VDDIO2 = 3V[2]	25 °C	0.5308	TBD	1.03	TBD	0.01341	TBD	µA	
		70 °C	0.785	TBD	4.81	TBD	0.3333	TBD		
		85 °C	1.210	TBD	9.80	TBD	0.84407	TBD		
		105 °C	1.760	TBD	25.41	TBD	2.56000	TBD		

1. ALL RAM Enabled.
2. The following bits were set: CORELPCNFG_ALLREFEN, CORELPCNFG_POREN, CORELPCNFG_LPOEN, CORESC_RTCOVRIDE , CORESC_USBOVRIDE , CORESC_VDDIOOVRIDE.

Table 69. Low power mode RAM adders — typical value

Core	SRAM Array	Start address	End address	Size	25 °C	70 °C	85 °C	105 °C	Unit
CPU0	ITCM0	0x0800_0000	0x0800_1FFF	8 KB	TBD	TBD	TBD	TBD	µA
	ITCM1	0x0800_2000	0x0800_3FFF	8 KB	TBD	TBD	TBD	TBD	µA
	ITCM2	0x0800_4000	0x0800_7FFF	16 KB	TBD	TBD	TBD	TBD	µA
	ITCM3	0x0800_8000	0x0800_FFFF	32 KB	TBD	TBD	TBD	TBD	µA
	DTCM0	0x2000_0000	0x2000_1FFF	8 KB	TBD	TBD	TBD	TBD	µA
	DTCM1	0x2000_2000	0x2000_3FFF	8 KB	TBD	TBD	TBD	TBD	µA

Table continues on the next page...

Table 69. Low power mode RAM adders — typical value (continued)

Core	SRAM Array	Start address	End address	Size	25 °C	70 °C	85 °C	105 °C	Unit
	DTCM2	0x2000_4000	0x2000_7FFF	16 KB	TBD	TBD	TBD	TBD	µA
	DTCM3	0x2000_8000	0x2000_FFFF	32 KB	TBD	TBD	TBD	TBD	µA
	DTCM4	0x2001_0000	0x2001_7FFF	32 KB	TBD	TBD	TBD	TBD	µA
	DTCM5	0x2001_8000	0x2001_FFFF	32 KB	TBD	TBD	TBD	TBD	µA
	DTCM6	0x2002_0000	0x2002_7FFF	32 KB	TBD	TBD	TBD	TBD	µA
	DTCM7	0x2002_8000	0x2002_FFFF	32 KB	TBD	TBD	TBD	TBD	µA
CPU1	TCM0	0x0900_0000	0x0900_1FFF	8 KB	TBD	TBD	TBD	TBD	µA
	TCM1	0x0900_2000	0x0900_3FFF	8 KB	TBD	TBD	TBD	TBD	µA
	TCM2	0x0900_4000	0x0900_7FFF	16 KB	TBD	TBD	TBD	TBD	µA
	TCM3	0x0900_8000	0x0900_FFFF	32 KB	TBD	TBD	TBD	TBD	µA
	TCM4	0x0901_0000	0x0901_7FFF	32 KB	TBD	TBD	TBD	TBD	µA
	TCM5	0x0901_8000	0x0901_FFFF	32 KB	TBD	TBD	TBD	TBD	µA

4.3.2.6 EMC radiated emissions operating behaviors

EMC measurements to IC-level IEC standards are available from NXP on request.

4.3.2.7 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to nxp.com.
2. Perform a keyword search for “EMC design”.

4.3.2.8 Capacitance attributes

Table 70. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN}	Input capacitance	—	7	pF

4.3.3 Switching specifications

4.3.3.1 Device clock specifications

Table 71. Device clock specifications

Symbol	Description	Min.	Max.	Unit	Run mode[1]
Normal run mode					
f_{CORE}	Core clock (DIVCORE)	—	72	MHz	High speed run mode
		—	48	MHz	Normal speed run mode
		—	8	MHz	VLPR mode
f_{EXT}	External clock (DIVEXT)	—	72	MHz	High speed run mode
		—	48	MHz	Normal speed run mode
		—	8	MHz	VLPR mode
f_{BUS}	Bus clock (DIVBUS)	—	72	MHz	High speed run mode
		—	48	MHz	Normal speed run mode
		—	8	MHz	VLPR mode
f_{SLOW}	Slow clock (DIVSLOW)	—	24	MHz	High speed run mode
		—	24	MHz	Normal speed run mode
		—	1	MHz	VLPR mode
f_{LLWU}	LLWU clock	—	1	KHz	All modes
f_{WDOG}	WDOG clock	—	24	MHz	High speed run mode and Normal speed run mode
		—	1	MHz	VLPR mode
f_{ADC}	ADC clock	—	48[2]	MHz	High speed run mode and Normal speed run mode
		—	8	MHz	VLPR mode
f_{RTC}	RTC clock	—	32.768	KHz	All modes
f_{TSTMR}	TSTMR clock	—	1	MHz	All modes
f_{LPTMR}	LPTMR clock	—	32[3]	MHz	All modes
f_{TPM}, f_{LPIT}, f_{LPSPI}, f_{LPI2C}, f_{LPUART}, f_{EMVSIM}, f_{I2S}, f_{FLEXIO}	TPM clock, LPIT clock, LPSPI clock, LPI2C clock, LPUART clock, EMVSIM clock, I2S clock, FlexIO clock	—	72	MHz	High speed run mode
		—	48	MHz	Normal speed run mode
		—	8	MHz	VLPR mode
f_{USB}	USB clock	—	48	MHz	High speed run mode and Normal speed run mode
		—	0	MHz	VLPR mode

Table continues on the next page...

Table 71. Device clock specifications (continued)

Symbol	Description	Min.	Max.	Unit	Run mode[1]
f_{ERCLK}	External reference clock	—	48	MHz	High speed run mode and Normal speed run mode
			8	MHz	VLPR mode
f_{RF_OSC}	Radio module output clock	—	32	MHz	High speed run mode and Normal speed run mode
		—	26	MHz	High speed run mode and Normal speed run mode
f_{CAU3}, f_{GPIO}, f_{uSDHC}, f_{TRNG}	CAU3 clock, GPIO clock, uSDHC clock	—	72	MHz	High speed run mode
		—	48	MHz	Normal speed run mode
		—	8	MHz	VLPR mode
f_{RADIO_ANA}	Radio analog module clock	—	24	MHz	High speed run mode and Normal speed run mode
		—	1	MHz	VLPR mode

1. Normal run mode, High speed run mode, and VLPR mode.
2. See ADC electrical specifications
3. The Max. of 32 MHz is from RF_OSC.

4.3.3.2 General switching specifications

These general-purpose specifications apply to all signals configured for GPIO, LPI2C, and LPUART signals.

NOTE

The term 'V_{DDIO}' in this table refers to the associated supply rail (either V_{DDIO1} or V_{DDIO2}) of an input or output.

Table 72. General switching specifications

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width (digital glitch filter disabled) — Synchronous path	1.5	—	Bus clock cycles	1
GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter enabled) — Asynchronous path	100	—	ns	
GPIO pin interrupt pulse width (digital glitch filter disabled, analog filter disabled) — Asynchronous path	50	—	ns	
External RESET and NMI pin interrupt pulse width — Asynchronous path	100	—	ns	2

Table continues on the next page...

Table 72. General switching specifications (continued)

Description	Min.	Max.	Unit	Notes
GPIO pin interrupt pulse width — Asynchronous path	16	—	ns	2
Port rise/fall time				
Normal drive pins				3
• 2.7 ≤ V_{DDIO} ≤ 3.6 V				
• Fast slew rate	—	3	ns	
• Slow slew rate	—	10.5		
• 1.71 ≤ V_{DDIO} ≤ 2.7 V				
• Fast slew rate	—	4		
• Slow slew rate	—	17		
High drive pins				4
Normal/low drive enabled				
• 2.7 ≤ V_{DDIO} ≤ 3.6 V				
• Fast slew rate	—	2.5	ns	
• Slow slew rate	—	10.5		
• 1.71 ≤ V_{DDIO} ≤ 2.7 V				
• Fast slew rate	—	4		
• Slow slew rate	—	17		
High drive enabled				
• 2.7 ≤ V_{DDIO} ≤ 3.6 V				
• Fast slew rate	—	2		
• Slow slew rate	—	11		
• 1.71 ≤ V_{DDIO} ≤ 2.7 V				
• Fast slew rate	—	2.5		
• Slow slew rate	—	17		
Normal drive fast pins				5
• 2.7 ≤ V_{DDIO} ≤ 3.6 V				
• Fast slew rate	—	0.5	ns	
• Slow slew rate	—	10		
• 1.71 ≤ V_{DDIO} ≤ 2.7 V				
• Fast slew rate	—	0.75		
• Slow slew rate	—	19		
High drive fast pins				6
Normal/low drive enabled				
• 2.7 ≤ V_{DDIO} ≤ 3.6 V				
• Fast slew rate	—	0.5	ns	
• Slow slew rate	—	11		
• 1.71 ≤ V_{DDIO} ≤ 2.7 V				
• Fast slew rate	—	1		
• Slow slew rate	—	19		
High drive enabled				
• 2.7 ≤ V_{DDIO} ≤ 3.6 V	—	2		

Table 72. General switching specifications

Description	Min.	Max.	Unit	Notes
• Fast slew rate • Slow slew rate	—	13		
• 1.71 ≤ V_{DDIO} ≤ 2.7 V • Fast slew rate • Slow slew rate	— —	4 21		

1. The synchronous and asynchronous timing must be met.
2. This is the shortest pulse that is guaranteed to be recognized.
3. For high drive pins with high drive enabled, load is 75pF; other pins load (normal/low drive) is 25pF. Fast slew rate is enabled by clearing PORTx_PCRn[SRE].
4. High drive pins are PTC[12:7], PTD[11:8], and PTE[11:10]. High drive capability is enabled by setting PORTx_PCRn[DSE].
5. Normal drive fast pins are PTD[7:2], PTE[12,9:8,5:1], PTB[2,0].
6. High drive fast pins are PTC[12:7], PTD[11:8], and PTE[11:10]. High drive capability is enabled by setting PORTx_PCRn[DSE].

NOTE

Only RESET_b pin has analog/passive filter.

4.3.4 Thermal specifications

4.3.4.1 Thermal operating requirements

Table 73. Thermal operating requirements for VFBGA package

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	125	°C	
T_A	Ambient temperature	–40	105	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times$ chip power dissipation.

Table 74. Thermal operating requirements for WLCSP package

Symbol	Description	Min.	Max.	Unit	Notes
T_J	Die junction temperature	–40	95	°C	
T_A	Ambient temperature	–40	85	°C	1

1. Maximum T_A can be exceeded only if the user ensures that T_J does not exceed the maximum. The simplest method to determine T_J is: $T_J = T_A + R_{\theta JA} \times$ chip power dissipation.

4.3.4.2 Thermal attributes

Table 75. Thermal attributes

Board type1[1]	Symbol	Description	176 VFBGA	191 WLCSP	Unit	Notes
JESD51-9,2s2p	$R_{\theta JA}$	Junction to Ambient Thermal Resistance	35.6	29.2	°C/W	2, 3
-	Ψ_{JT}	Junction to Package Top Thermal Resistance	0.2	0.4	°C/W	4, 3

1. Thermal test board meets JEDEC specification for this package (JESD51-9).
2. Determined in accordance to JEDEC JESD51-2A natural convection environment. Thermal resistance data in this report is solely for a thermal performance comparison of one package to another in a standardized specified environment. It is not meant to predict the performance of a package in an application-specific environment.
3. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the bard, and board construction.
4. Thermal characterization parameter indicating the temperature difference between the package top and the junction temperature per JEDEC JESD51-2.

The thermal characterization parameter (Psi-JT) can be used to determine the junction temperature with a measurement of the temperature at the top of the package case using the following equation:

$T_J = T_T$ + Psi-JT x chip power dissipation

Where T_T is the thermocouple temperature at the top of the package.

4.4 Peripheral operating requirements and behaviors

4.4.1 Core modules

4.4.1.1 Debug trace timing specifications

Table 76. Debug trace operating behaviors

Symbol	Description	Min.	Max.	Unit
T_{cyc}	Clock period	Frequency dependent		MHz
T_{wl}	Low pulse width	2	—	ns
T_{wh}	High pulse width	2	—	ns
T_r	Clock and data rise time	—	3	ns
T_f	Clock and data fall time	—	3	ns

Table continues on the next page...

Table 76. Debug trace operating behaviors (continued)

Symbol	Description	Min.	Max.	Unit
T_s	Data setup	1.5	—	ns
T_h	Data hold	1.0	—	ns

4.4.1.2 SWD electricals

Table 77. SWD full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	SWD_CLK frequency of operation • Serial wire debug	0	25	MHz
J2	SWD_CLK cycle period	1/J1	—	ns
J3	SWD_CLK clock pulse width • Serial wire debug	20	—	ns
J4	SWD_CLK rise and fall times	—	3	ns
J9	SWD_DIO input data setup time to SWD_CLK rise	10	—	ns
J10	SWD_DIO input data hold time after SWD_CLK rise	0	—	ns
J11	SWD_CLK high to SWD_DIO data valid	—	32	ns
J12	SWD_CLK high to SWD_DIO high-Z	5	—	ns

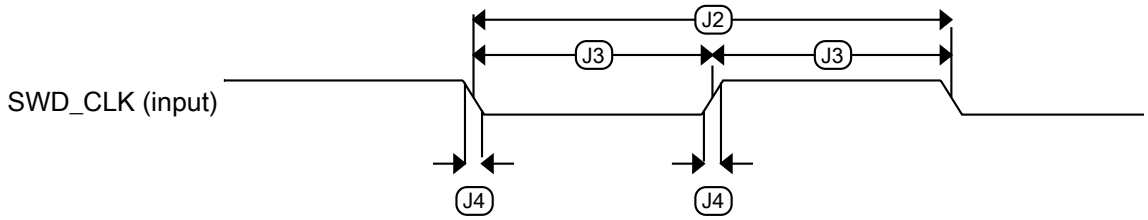


Figure 11. Serial wire clock input timing

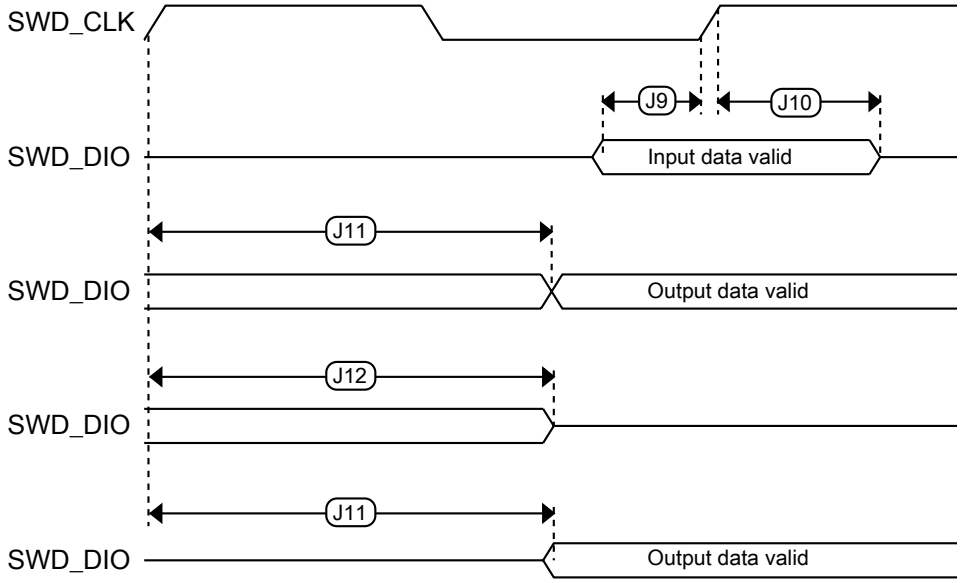


Figure 12. Serial wire data timing

4.4.1.3 JTAG electricals

Table 78. JTAG limited voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	2.7	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	20	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	25	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1	—	ns

Table continues on the next page...

Table 78. JTAG limited voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J11	TCLK low to TDO data valid	—	19	ns
J12	TCLK low to TDO high-Z	—	19	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

Table 79. JTAG full voltage range electricals

Symbol	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
J1	TCLK frequency of operation			MHz
	• Boundary Scan	0	10	
	• JTAG and CJTAG	0	15	
J2	TCLK cycle period	1/J1	—	ns
J3	TCLK clock pulse width			
	• Boundary Scan	50	—	ns
	• JTAG and CJTAG	33	—	ns
J4	TCLK rise and fall times	—	3	ns
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	1.4	—	ns
J7	TCLK low to boundary scan output data valid	—	27	ns
J8	TCLK low to boundary scan output high-Z	—	27	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	26.2	ns
J12	TCLK low to TDO high-Z	—	26.2	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

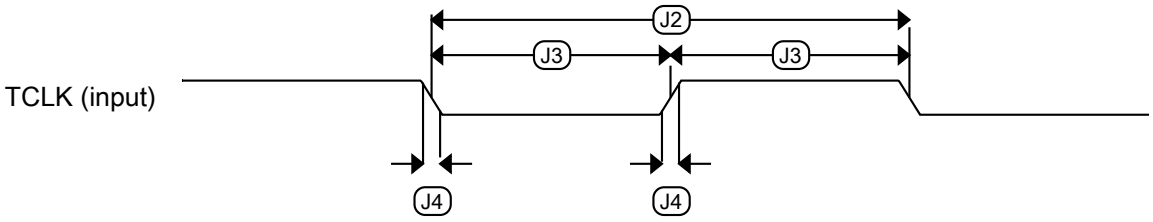


Figure 13. Test clock input timing

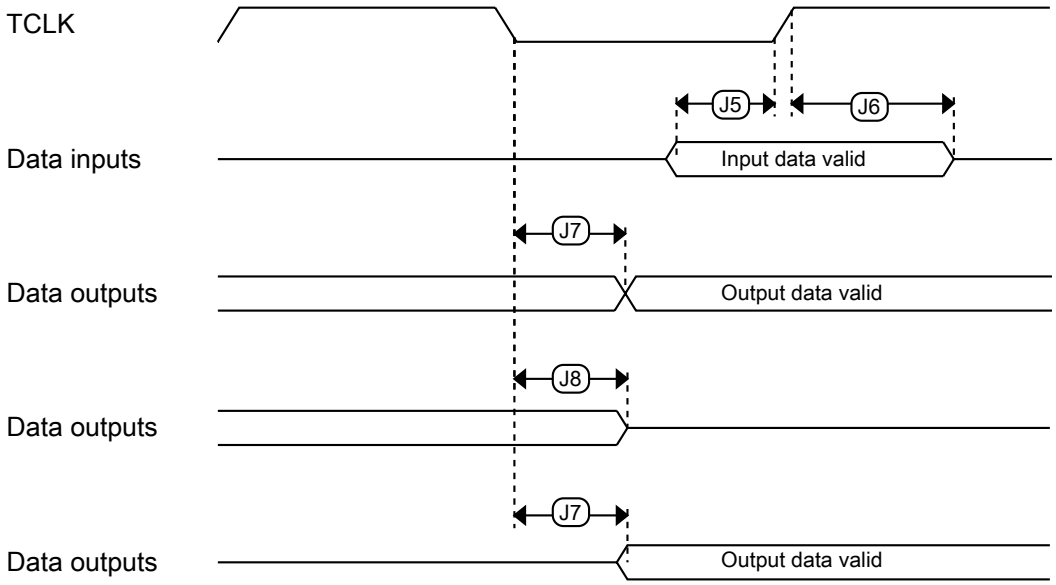


Figure 14. Boundary scan (JTAG) timing

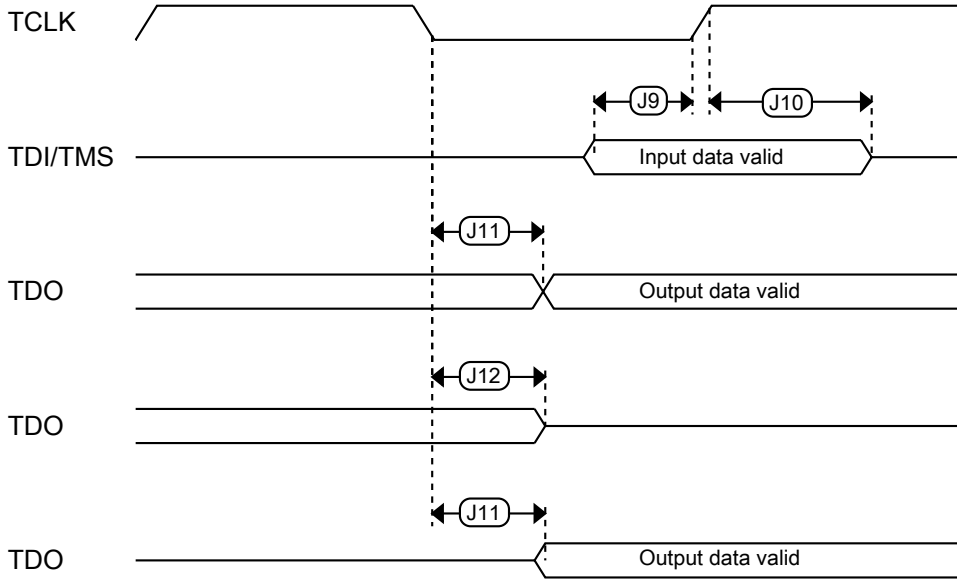


Figure 15. Test Access Port timing

4.4.2 System modules

There are no specifications necessary for the device's system modules.

4.4.3 Clock modules

4.4.3.1 Clock modules

4.4.3.1.1 Fast IRC (FIRC) specifications

Table 80. Fast IRC (FIRC) specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{dd_firc}	Supply voltage	1.71	—	3.6	V	
F_{firc_target}	IRC target frequency (nominal) Trim range = 00 Trim range = 01 Trim range = 10 Trim range = 11	—	 48 52 56 60	—	MHz	1
$\Delta f_{firc\_ol\_lv}$	Open loop total deviation of FIRC frequency at low voltage (VDD=1.71V-1.89V) over full temperature • Regulator disable (SCG_FIRCCSR[FIRCREGOFF]=1) • Regulator enable (SCG_FIRCCSR[FIRCREGOFF]=0)	—	±0.5 ±0.5	±1.5 ±1.5	$\%F_{firc\_target}$	
$\Delta f_{firc\_48M\_ol\_hv}$	Open loop total deviation of FIRC frequency at high voltage (VDD=1.89V-3.6V) over full temperature Regulator enable (SCG_FIRCCSR[FIRCREGOFF]=0)	—	±0.5	±1.0	$\%F_{firc\_target}$	2
$\Delta f_{firc\_60M\_ol\_hv}$	Open loop total deviation of FIRC frequency at high voltage (VDD=1.89V-3.6V) over full temperature Regulator enable (SCG_FIRCCSR[FIRCREGOFF]=0)	—	±0.5	±1.5	$\%F_{firc\_target}$	2
Δf_{firc_cl}	Fine Trim Resolution	—	—	± 0.1	$\%F_{firc\_target}$	
J_{cyc_firc}	Period Jitter (RMS)	—	35	150	ps	
T_{st_firc}	Startup time	—	2	3	µs	3
I_{dd_firc}	Current consumption: • 48 MHz • 52 MHz • 56 MHz • 60 MHz	 — — — —	 350 360 380 400	 400 420 460 500	µA	

1. FIRC trim range is programmable via SCG_FIRCCFG[RANGE].
2. Closed loop operation of the FIRC is only usable for USB device operation; it is not usable for USB host operation. It is enabled by configuring for USB Device, selecting FIRC as USB clock source, and enabling the clock recover function (USB_CLK_RECOVER_CTRL[CLOCK_RECOVER_EN]=1, SCG_FIRCCSR[FIRCREGOFF]=0).
3. FIRC startup time is defined as the time between clock enablement and clock availability for system use.

4.4.3.1.2 Slow IRC (SIRC) specifications

Table 81. Slow IRC specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DD_sirc2M}	Supply current in 2 MHz mode	—	14	17	µA	
I_{DD_sirc8M}	Supply current in 8 MHz mode	—	25	35	µA	
f_{sirc}	Output frequency	—	2	—	MHz	1
		—	8	—		
Δf_{sirc}	Total deviation of trimmed frequency over voltage and temperature	—	—	±3.3	$\%f_{sirc}$	
Δf_{sirc_t}	Total deviation of trimmed frequency over voltage and reduced temperature range from -20 ºC to 105 ºC	—	—	3	$\%f_{sirc}$	
T_{su_sirc}	Startup time	—	—	12.5	µs	
J_{cyc_sirc}	Period jitter (RMS) • f_{sirc} = 2 MHz • f_{sirc} = 8 Mhz	— —	350 100	— —	ps	2

1. Selection of output frequency for Slow IRC between 2 MHz and 8 MHz is controlled by SCG_ SIRCCFG[RANGE].
2. This specification was obtained using an NXP developed PCB. Jitter is dependent on the noise characteristics of each PCB and results will vary.

4.4.3.1.3 Low Power Oscillator (LPO) electrical specifications

Table 82. Low Power Oscillator (LPO) electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
F_{LPO}	Internal low power oscillator frequency	0.9	1	1.1	kHz
I_{LPO}	Current consumption	—	8.85	TBD	µA
$T_{startup}$	Startup Time	—	—	TBD	µs

4.4.3.1.4 LPFLL electrical specifications

Table 83. LPFLL electrical specifications

Symbol	Parameter	Min.	Typ.	Max.	Unit
I_{avg}	Power consumption		240		µA

Table continues on the next page...

Table 83. LPFLL electrical specifications (continued)

Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{start}	Start-up time		3.6		µs
ΔF_{ol}	Frequency accuracy over temperature and voltage in open loop after process trimmed	–10	—	10	%
ΔF_{cl}	Frequency accuracy in closed loop	–1 [1]	—	1 [1]	%

1. ΔF_{cl} is dependent on reference clock accuracy. For example, if locked to crystal oscillator, ΔF_{cl} is typically limited by trimming ability of the module itself; if locked to other clock source which has 3% accuracy, then ΔF_{cl} can only be ±3%.

4.4.3.2 32 kHz oscillator electrical characteristics

4.4.3.2.1 32 kHz oscillator DC electrical specifications

Table 84. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp} [1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

4.4.3.2.2 32 kHz oscillator frequency specifications

Table 85. 32 kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$f_{ec\_extal32}$	Externally provided input clock frequency	—	32.768	—	kHz	2
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

4.4.3.3 Recommended crystal and oscillator specification

This chip is designed to meet targeted standard specifications for frequency error over the life of the part, which includes the temperature, mechanical and aging effects.

The table below includes the recommended crystal specifications. Note that these are recommendations only and deviation may be allowed. However, deviations may result in degraded RF performance or possibly a failure to meet RF protocol certification standards. Designers must ensure that the crysta(s) used meets the requirements of their application.

Table 86. Recommended crystal and oscillator specification

Symbol	Description	32.0 MHz			26.0 MHz			Unit	Note
		Min	Typ	Max	Min	Typ	Max		
T_A	Operating Temperature	-40		105	-40		105	℃	1
	Crystal initial frequency tolerance	-10		10	-10		10	ppm	2, 3
	Crystal frequency stability and aging	-25		25	-25		24	ppm	2, 4
	Oscillator variation	-12		15	-12		16	ppm	5
	Total reference oscillator tolerance for BLE applications	-50		50	-50		50	ppm	6
C_L	Load capacitance	7	10	13	7	10	13	pF	2, 7
C_0	Shunt capacitance	0.469	0.67	0.871	0.42	0.6	0.78	pF	2, 7
C_{m1}	Motional capacitance	1.435	2.05	2.665	1.435	2.05	2.665	fF	2, 7
L_{m1}	Motional inductance Lm1	8.47	12.1	15.73	12.81	18.3	23.79	mH	2, 7
R_{m1}	Motional resistance		25	50		35	50	Ω	2
ESR	Equivalent series resistance			60			60	Ω	
Pd	Maximum crystal drive		10	200		10	200	µw	2
TS	Trim sensitivity	6.30	9.00	11.70	6.39	9.12	11.86	ppm/pF	2, 7
T_{OSC}	Oscillator startup time		500			500		µs	8

1. Full temperature range of this device. A reduced range can be chosen to meet application needs.
2. Recommended crystal specification.
3. Measured at 25 ºC.

4. Combination of frequency stability variation over desired temperature range and frequency variation due to aging over desired lifetime of system.
5. Variation due to temperature, process, and aging of MCU.
6. Sum of crystal initial frequency tolerance, crystal frequency stability and aging, oscillator variation, and PCB manufacturing variation must not exceed this value.
7. Typical is target. 30% tolerances shown.
8. Time from oscillator enable to clock ready. Dependent on the complete hardware configuration of the oscillator.

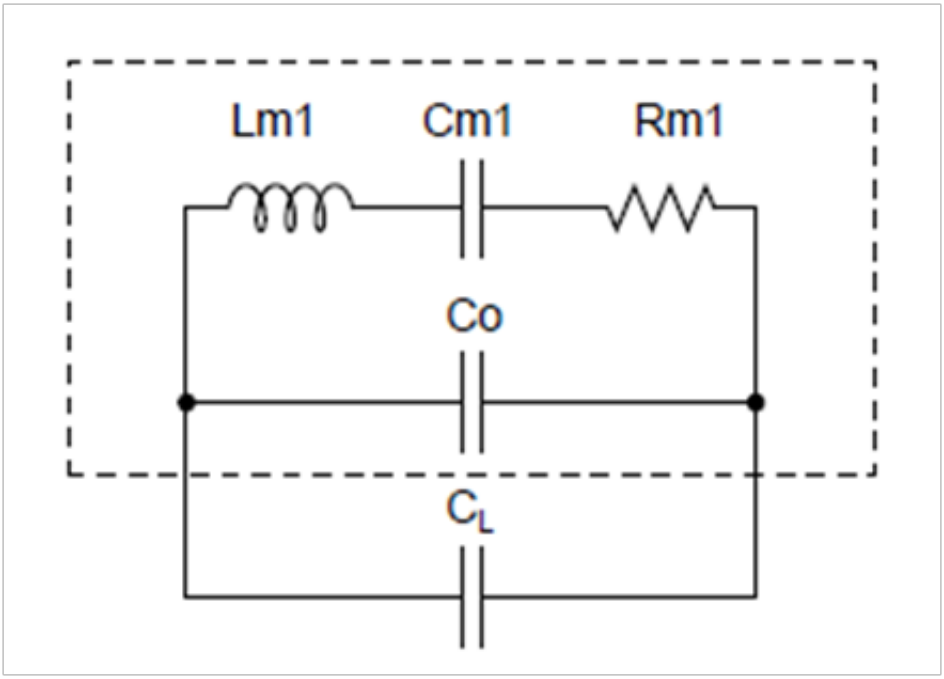


Figure 16. Crystal Electrical Block Diagram

4.4.4 Memories and memory interfaces

4.4.4.1 Flexbus switching specifications

All processor bus timings are synchronous; input setup/hold and output delay are given in respect to the rising edge of a reference clock, FB_CLK. The FB_CLK frequency may be the same as the internal system bus frequency or an integer divider of that frequency.

The following timing numbers indicate when data is latched or driven onto the external bus, relative to the Flexbus output clock (FB_CLK). All other timing relationships can be derived from these values.

Table 87. Flexbus limited voltage range switching specifications

Num	Description	Min.	Max.	Unit	Notes
	Frequency of operation	—	24	MHz	
FB1	Clock period	1/FB_CLK	—	ns	
FB2	Address, data, and control output valid	—	7	ns	
FB3	Address, data, and control output hold	1	—	ns	1
FB4	Data and $\overline{\text{FB\_TA}}$ input setup	7.2	—	ns	
FB5	Data and $\overline{\text{FB\_TA}}$ input hold	0	—	ns	2

1. Specification is valid for all FB_AD[31:0], $\overline{\text{FB\_BE}}$/BWE*n*, $\overline{\text{FB\_CS}}$*n*, $\overline{\text{FB\_OE}}$, FB_R/$\overline{\text{W}}$, $\overline{\text{FB\_TBST}}$, FB_TSIZ[1:0], FB_ALE, and $\overline{\text{FB\_TS}}$.
2. Specification is valid for all FB_AD[31:0] and $\overline{\text{FB\_TA}}$.

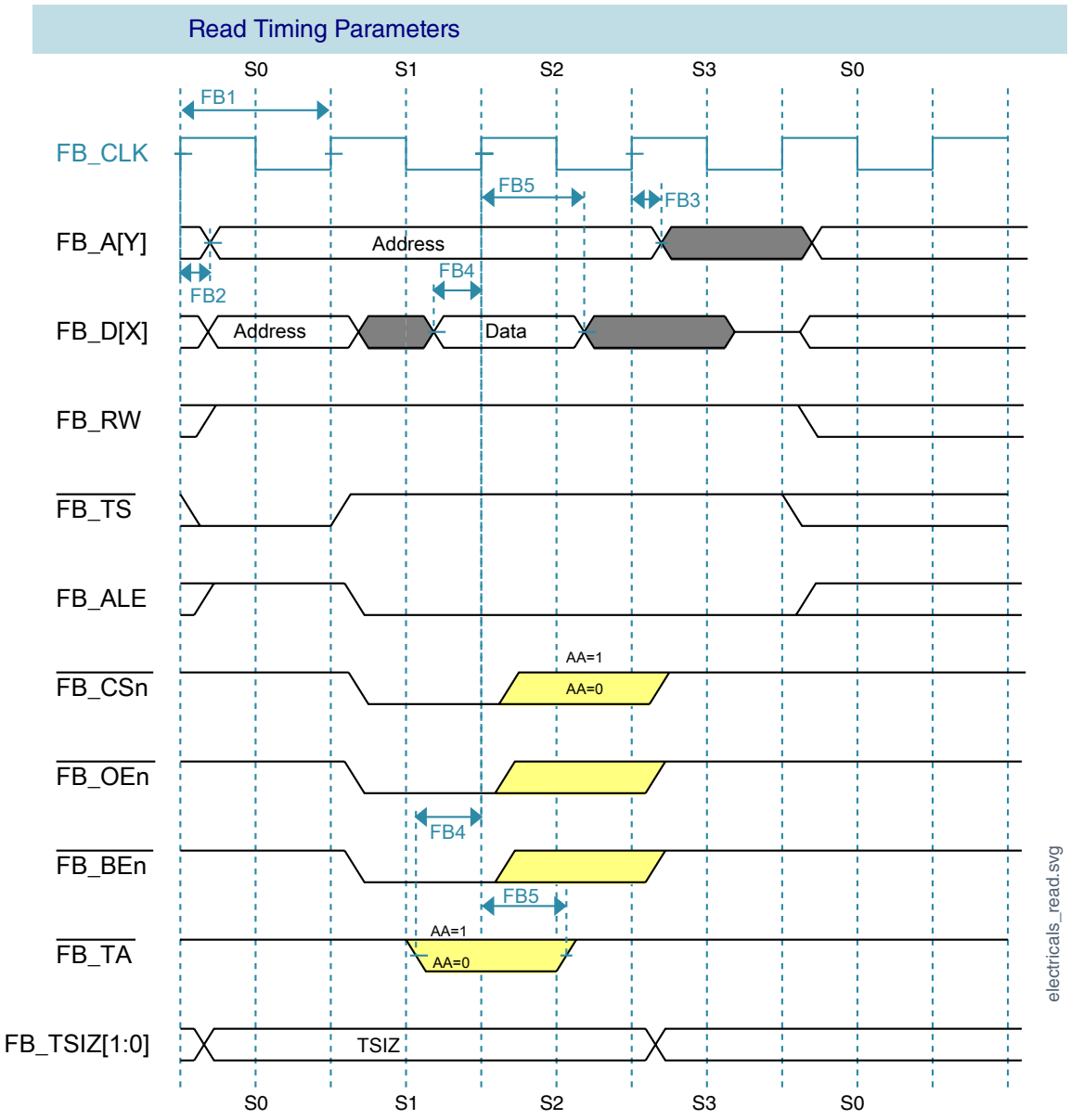


Figure 17. FlexBus read timing diagram

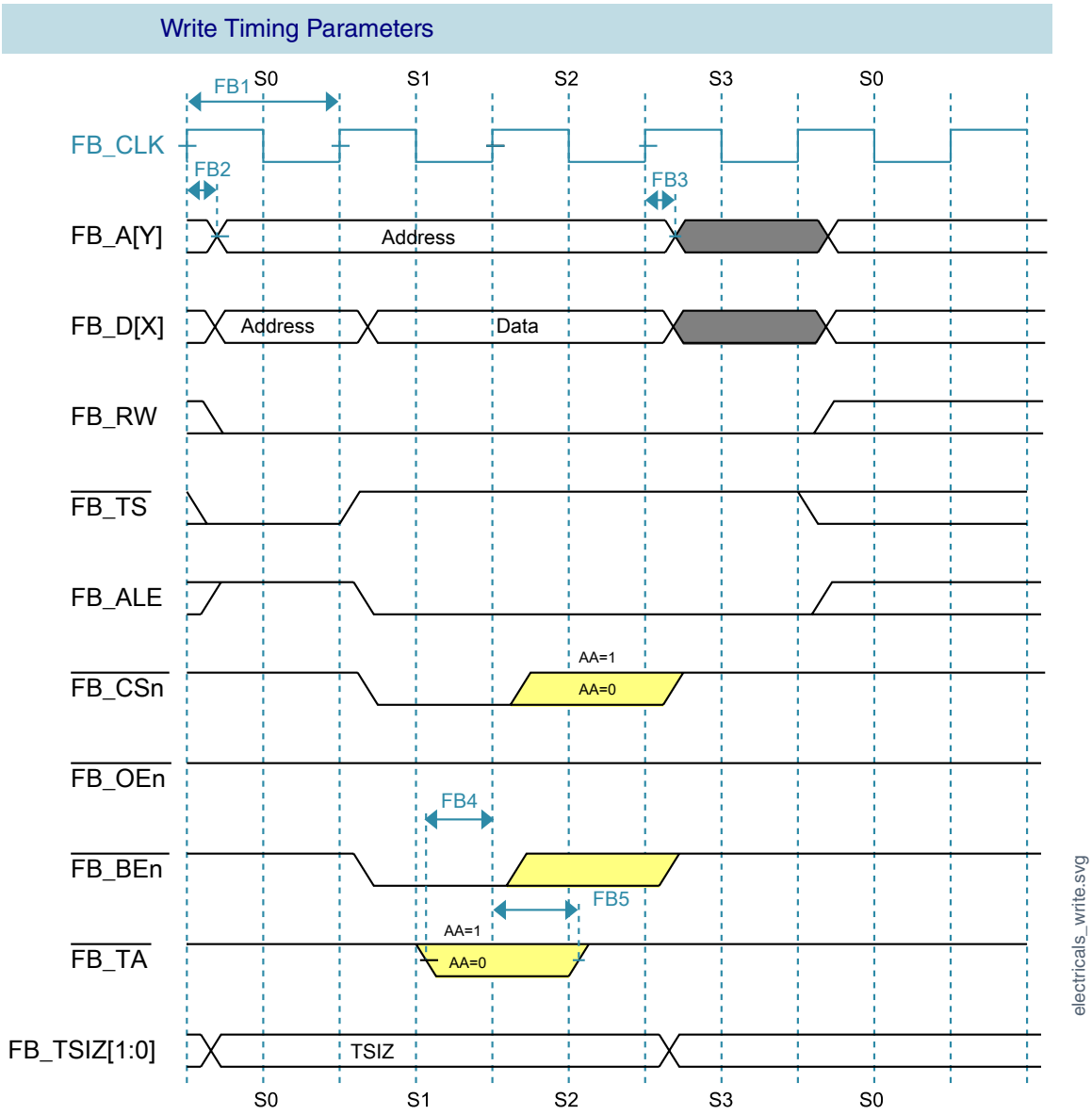


Figure 18. FlexBus write timing diagram

4.4.4.2 Ultra High Speed SD/SDIO/MMC Host Interface (uSDHC) AC timing

This section describes the electrical information of the uSDHC, which includes SD/eMMC4.3 (Single Data Rate) timing, eMMC4.4/4.41/4.5 (Dual Date Rate) timing

4.4.4.2.1 SD/eMMC4.3 (Single Data Rate) AC Timing

The following figure depicts the timing of SD/eMMC4.3

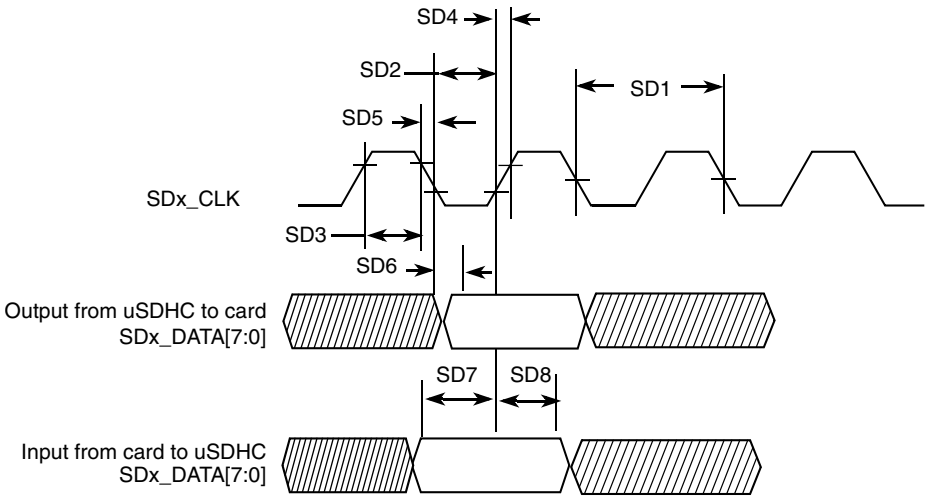


Figure 19. SD/eMMC4.3 timing

The following table lists the SD/eMMC4.3 timing characteristics.

Table 88. SD/eMMC4.3 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (Low Speed)	f_{PP}[1]	0	400	kHz
	Clock Frequency (SD/SDIO Full Speed/High Speed)	f_{PP}[2]	0	24/48	MHz
	Clock Frequency (MMC Full Speed/ High Speed)	f_{PP}[3]	0	16/48	MHz
	Clock Frequency (Identification Mode)	f_{OD}	100	400	kHz
SD2	Clock Low Time	t_{WL}	7	—	ns
SD3	Clock High Time	t_{WH}	7	—	ns
SD4	Clock Rise Time	t_{TLH}	—	3	ns
SD5	Clock Fall Time	t_{THL}	—	3	ns
uSDHC Output/Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD6	uSDHC Output Delay	t_{OD}	-6.6	3.6	ns
uSDHC Input/Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD7	uSDHC Input Setup Time	t_{ISU}	2.5	—	ns
SD8	uSDHC Input Hold Time[4]	t_{IH}	1.5	—	ns

1. In low speed mode, card clock must be lower than 400 kHz, voltage ranges from 2.7 to 3.6 V.

2. In normal (full) speed mode for SD/SDIO card, clock frequency can be any value between 0–24 MHz. In high-speed mode, clock frequency can be any value between 0–48 MHz.
3. In normal (full) speed mode for MMC card, clock frequency can be any value between 0–16 MHz. In high-speed mode, clock frequency can be any value between 0–48 MHz.
4. To satisfy hold timing, the delay difference between clock input and cmd/data input must not exceed 2 ns.

4.4.4.2.2 eMMC4.4/4.41 (Dual Data Rate) AC Timing

The following figure depicts the timing of eMMC4.4/4.41.

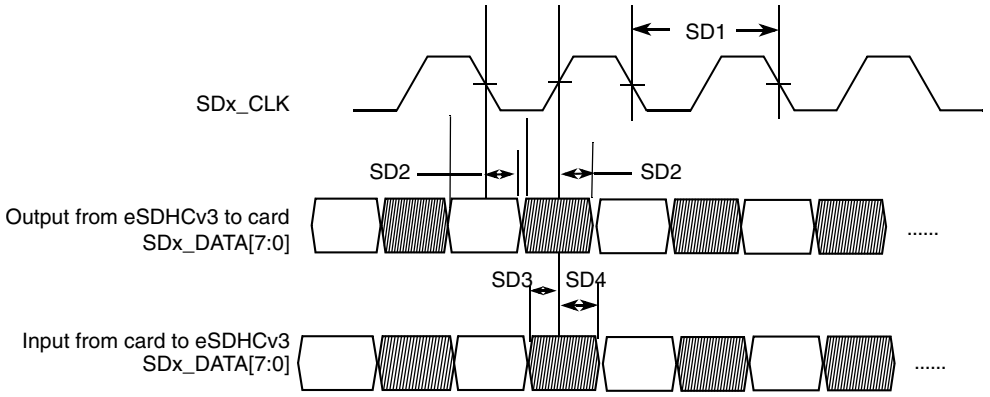


Figure 20. eMMC4.4/4.41 timing

The following table lists the eMMC4.4/4.41 timing characteristics. Be aware that only DATA is sampled on both edges of the clock (not applicable to CMD).

Table 89. eMMC4.4/4.41 interface timing specification

ID	Parameter	Symbols	Min	Max	Unit
Card Input Clock					
SD1	Clock Frequency (eMMC4.4/4.41 DDR)	f_{PP}	0	52	MHz
SD1	Clock Frequency (SD3.0 DDR)	f_{PP}	0	50	MHz
uSDHC Output / Card Inputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD2	uSDHC Output Delay	t_{OD}	2.5	7.1	ns
uSDHC Input / Card Outputs SD_CMD, SDx_DATAx (Reference to CLK)					
SD3	uSDHC Input Setup Time	t_{ISU}	2.6	—	ns
SD4	uSDHC Input Hold Time	t_{LH}	1.5	—	ns

4.4.4.3 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

4.4.4.3.1 Flash timing specifications — commands

Table 90. Flash command timing specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Read 1s Block execution time					
$t_{rd1blk256k}$	256 KB secondary program flash	—	—	2	ms	
$t_{rd1blk512k}$	512 KB primary program flash	—	—	2	ms	
	Read 1s Section execution time					
$t_{rd1sec2k}$	2 KB flash	—	—	90	µs	1
$t_{rd1sec4k}$	4 KB flash	—	—	100	µs	1
t_{pgmchk}	Program Check execution time	—	—	95	µs	1
t_{pgm8}	Program Phrase execution time	—	110	225	µs	
	Erase Flash Block execution time					2
$t_{ersblk256k}$	256 KB secondary program flash	—	220	2500	ms	
$t_{ersblk512k}$	512 KB primary program flash	—	435	5000	ms	
t_{ersscr}	Erase Flash Sector execution time	—	15	150	ms	2
$t_{pgmsec1k}$	Program Section execution time (1KB flash)	—	8	—	ms	
	Generate CRC execution time (CRCRDY=0)					
t_{crc4}	4 sectors	—	375	425	µs	
t_{crc32}	32 sectors	—	3	3.5	ms	
t_{crc128}	128 sectors	—	12	14	ms	
	Generate CRC execution time (CRCRDY=1)					
t_{crcr4}	4 sectors	—	860	985	µs	
t_{crcr32}	32 sectors	—	7	8	ms	
$t_{crcr128}$	128 sectors	—	28	32	ms	
$t_{rd1allx}$	Read 1s All Blocks execution time	—	—	6	ms	
$t_{rdindex}$	Read Index execution time	—	—	35	µs	1
$t_{pgmindex}$	Program Index execution time	—	110	—	µs	
t_{ersall}	Erase All Blocks execution time	—	1100	13000	ms	2
t_{vfykey}	Verify Backdoor Access Key execution time	—	—	40	µs	1
	Swap Control execution time					
$t_{swapx01}$	control code 0x01	—	350	—	µs	
$t_{swapx02}$	control code 0x02	—	125	250	µs	
$t_{swapx04}$	control code 0x04	—	150	275	µs	
$t_{swapx08}$	control code 0x08	—	—	40	µs	1
$t_{swapx10}$	control code 0x10	—	125	250	µs	
$t_{ersallu}$	Erase All Blocks Unsecure execution time	—	1100	13000	ms	2

Table continues on the next page...

Table 90. Flash command timing specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
	Set RAM Function execution time					
$t_{setramcc}$	Control Code 0xCC	—	130	—	µs	
$t_{setramff}$	Control Code 0xFF	—	85	—	µs	

1. Assumes 25MHz or greater flash clock frequency.
2. Maximum times for erase parameters based on expectations at cycling end-of-life.

4.4.4.3.2 Flash high voltage current behaviors

Table 91. Flash high voltage current behaviors

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DD_PGM}	Average current adder during high voltage flash programming operation	—	3.5	7.5	mA
I_{DD_ERS}	Average current adder during high voltage flash erase operation	—	1.5	4.0	mA

4.4.4.3.3 Reliability specifications

Table 92. NVM reliability specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
	Program Flash					
$t_{nvmretp10k}$	Data retention after up to 10 K cycles	5	50	—	years	
$t_{nvmretp1k}$	Data retention after up to 1 K cycles	20	100	—	years	
$n_{nvmcycp}$	Cycling endurance	10 K	50 K	—	cycles	2

1. Typical data retention values are based on measured response accelerated at high temperature and derated to a constant 25°C use profile. Engineering Bulletin EB618 does not apply to this technology. Typical endurance defined in Engineering Bulletin EB619.
2. Cycling endurance represents number of program/erase cycles at -40°C ≤ T_j ≤ 125°C.

4.4.5 Security and integrity modules

There are no specifications necessary for the device's security and integrity modules.

4.4.6 Analog

4.4.6.1 ADC electrical specifications

4.4.6.1.1 ADC operating conditions

Table 93. ADC operating conditions

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
V_{DDA}	Supply voltage		1.71	—	3.6	V	2
V_{REFH}	ADC reference voltage high		1.2	—	V_{DDA}	V	
V_{REFL}	ADC reference voltage low		V_{SSA}	V_{SSA}	V_{SSA}	V	
V_{ADIN}	Input voltage		VREFL	—	Min. of VREFH and VDDIOx[3]	V	4
C_{ADIN}	Input capacitance	• 12-bit mode	—	5	7	pF	
R_{ADIN}	Input series resistance		—	2	5	kΩ	
R_{AS}	Analog source resistance (external)	12-bit mode f_{ADCK} < TBD MHz	—	—	5	kΩ	5
f_{ADCK}	ADC conversion clock frequency	12-bit mode • CFG[PWRSEL]=0b00 • CFG[PWRSEL]=0b01 • CFG[PWRSEL]=0b10 • CFG[PWRSEL]=0b11	 4 4 4 4	 — — — —	 4 8 16 32	MHz	
C_{rate}	ADC conversion rate	12-bit mode, no ADC hardware averaging • CFG[PWRSEL]=0b00 • CFG[PWRSEL]=0b01 • CFG[PWRSEL]=0b10 • CFG[PWRSEL]=0b11	 234.771 234.939 234.853 234.936	 — — — —	 235.546 472.322 248.294 1230.830	ksps	
$t_{ADCSTUP}$	Analog startup time		—	—	4	µs	6

1. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz, unless otherwise stated. Typical values are for reference only, and are not tested in production.
2. V_{DDA} must be equal to the higher of V_{DDIO1} or V_{DDIO2}.
3. VDDIOx is either VDDIO1 or VDDIO2 and is dependent on the IO supply associated with the ADC channel pin. If VREFH is less than VDDIOx, then voltage inputs greater than VREFH but less than VDDIOx are allowed but result in a saturated conversion result.
4. If VREFH is less than VDDA, then voltage inputs greater than VREFH but less than VDDA are allowed but result in a saturated conversion result.

5. This resistance is external to the packaged device. To achieve the best results, the analog source resistance must be kept as low as possible. The results in this data sheet were derived from a system that had < 8 Ω analog source resistance. The $R_{AS} \times C_{AS}$ time constant should be kept to < 1 ns.
6. The startup time is defined as the duration from when (1) CFG[PWREN] is set or (2) when a trigger event initiates command execution until the analog circuits are stable and ready to sample and convert analog input channels. When CFG[PWREN]=0b0, the delay period controlled by CFG[PUDLY] after an initial trigger detect must exceed the analog startup time of $t_{ADCSTUP}$ to guarantee ADC operation.

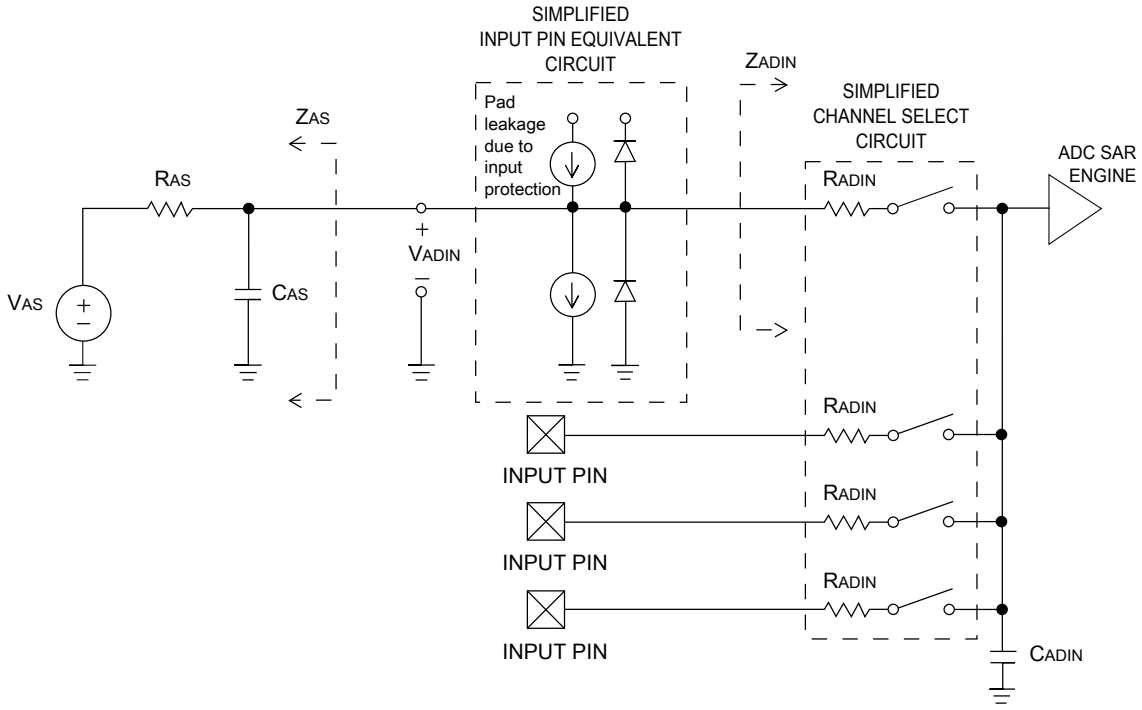


Figure 21. ADC input impedance equivalency diagram

4.4.6.1.2 ADC electrical characteristics

Table 94. ADC characteristics (V_{REFH} = TBD V, V_{REFL} = V_{SSA})

Symbol	Description	Conditions[1]	Min.	Typ. [2]	Max.	Unit	Notes
I_{DDA_ADC}	Supply current	CFG[PWRSEL]=0b00, f_{ADCK} = 4 MHz	—	40	—	µA	3
		CFG[PWRSEL]=0b01, f_{ADCK} = 12 MHz	—	95	—	µA	
		CFG[PWRSEL]=0b10, f_{ADCK} = 24 MHz	—	190	—	µA	
		CFG[PWRSEL]=0b11, f_{ADCK} = 48 MHz	—	380	—	µA	
I_{DDA_ADC}	Supply current	ADC Idle, analog pre-enabled (CFG[PWREN]=0b1)	—	10	—	µA	
I_{DDA_ADC}	Supply current	During ADC command execution	0.215	—	1.7	mA	4

Table continues on the next page...

Table 94. ADC characteristics (V_{REFH} = TBD V, V_{REFL} = V_{SSA}) (continued)

Symbol	Description	Conditions[1]	Min.	Typ. [2]	Max.	Unit	Notes
f_{ADACK}	ADC asynchronous clock source		—	2	—	MHz	
Δf_{ADACK_T}	Deviation of ADACK clock due to temperature		—	±7%	—		
	Sample Time	See Reference Manual chapter for sample times					
TUE	Total unadjusted error	• 12-bit mode	—	±4	±6.8	LSB[5]	6
DNL	Differential non-linearity	• 12-bit mode	—	±0.7	–1.1 to +1.9	LSB[5]	6
INL	Integral non-linearity	• 12-bit mode	—	±1.0	–2.7 to +1.9	LSB[5]	6
E_{FS}	Full-scale error	• 12-bit mode	—	–4	–5.4	LSB[5]	V_{ADIN} = V_{REFH}[6]
E_Q	Quantization error	• 12-bit mode	—	—	±0.5	LSB[5]	
ENOB	Effective number of bits	12-bit single-ended mode • Avg = 32 • Avg = 4	 — —	 9.561 10.014	 — —	 bits bits	7
E_{IL}	Input leakage error		$I_{In} \times R_{AS}$			mV	8
	Temp sensor slope	Across the full temperature range of the device	1.70	1.78	1.85	mV/°C	9
V_{TEMP25}	Temp sensor voltage	25 °C	701	711	721	mV	9

1. All accuracy numbers assume the ADC is calibrated with V_{REFH} = TBD V
2. Typical values assume V_{DDA} = 3.0 V, Temp = 25 °C, f_{ADCK} = 2.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.
3. Shortest sample time (CMDH*a*[STS]=0x0), continuous operation (command execution set for single or multi-command sequential loop).
4. The ADC supply current during command execution depends on the ADC conversion clock speed, power option selected (CFG[PWRSEL]) and sample time selected (CMDH*a*[STS]). For lowest power operation, set CFG[PWRSEL]=0b00 with TBD MHz ADC conversion clock speed. If the application allows slower conversion rates, longer sample times can be configured to reduce average power consumption.
5. 1 LSB = $(V_{REFH} - V_{REFL})/2^N$
6. ADC conversion clock < 16...TBD MHz, Max hardware averaging (CMDH*a*[AVGS] = 0x7)
7. Input data is 100 Hz sine wave. ADC conversion clock < 12 MHz.
8. I_{In} = leakage current. Refer to pin leakage specification in the packaged device's voltage and current operating ratings.
9. ADC conversion clock < 3 MHz

Figure 22. TBD PLACEHOLDER -- Typical ENOB vs. ADCK for 12-bit single-ended mode

4.4.6.2 Voltage reference electrical specifications

Table 95. VREF full-range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage for 1.2V output	1.71	3.6	V	—
	Supply voltage for 2.1V output	2.4	3.6	V	—
T_A	Temperature	Operating temperature range of the device		°C	—
C_L	Output load capacitance	100		nF	1, 2

1. C_L must be connected to VREF_OUT if the VREF_OUT functionality is being used for either an internal or external reference.
2. The load capacitance should not exceed +/-25% of the nominal specified C_L value over the operating temperature range of the device.

Table 96. VREF full-range operating behaviors

Symbol	Description		Min.	Typ.	Max.	Unit	Notes
V_{out}	Voltage reference output with factory trim at nominal VDDA and temperature=25 °C	1.2 V range	1.19	1.195	1.2	V	1
		2.1 V range	2.091	2.1	2.109	V	1
V_{step}	Voltage reference trim step for 1.2 V output		—	0.5	—	mV	1
	Voltage reference trim step for 2.1 V output		—	1.0	—	mV	1
I_{bg}	Bandgap only current		—	60	80	µA	1
I_{lp}	Low-power buffer current		—	180	360	µA	1
I_{hp}	High-power buffer current		—	480	960	µA	1
ΔV_{LOAD}	Load regulation — current is ± 1.0 mA		—	±0.2	—	mV	1, 2
T_{stup}	Buffer startup time		—	—	100	µs	—
V_{vdrift}	Voltage drift for 1.2 V output (Vmax -Vmin across the full voltage range)		—	0.5	2	mV	1
	Voltage drift for 2.1 V output (Vmax -Vmin across the full voltage range)		—	0.9	3.5	mV	
V_{tdrift}	Temperature drift for 1.2 V output (Vmax -Vmin across the full temperature range)		—	2	15	mV	3
	Temperature drift for 2.1 V output (Vmax -Vmin across the full temperature range)		—	3.5	27	mV	

1. See the chip's Reference Manual for the appropriate settings of the VREF Status and Control register for V_{out} selection of 1.2 V or 2.1 V.
2. Load regulation voltage is the difference between the VREF_OUT voltage with no load vs. voltage with defined load
3. To get best performance of VREF temperature drift, VREF_SC[ICOMPEN] must be set.

4.4.6.3 CMP and 6-bit DAC electrical specifications

Table 97. Comparator and 6-bit DAC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{DD}[1]	Supply voltage	1.71	—	3.6	V
I_{DDHS}	Supply current, high-speed mode (EN=1, HPMD=1)	—	—	180	µA
I_{DDLS}	Supply current, normal mode (EN=1, HPMD=0, NPMD=0)	—	—	20	µA
I_{DDNS}	Supply current, nano mode (EN=1, HPMD=0, NPMD=1)	—	—	0.390	µA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[2]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[3]	—	—	40	µs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	µA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[4]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. For LPCMP0 $V_{DD} = V_{DDIO1}$; for LPCMP1, $V_{DD} = V_{DDIO2}$.
2. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}–0.6 V.
3. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to CMP_DACCR[DACEN], CMP_DACCR[VRSEL], CMP_DACCR[VOSEL], CMP_MUXCR[PSEL], and CMP_MUXCR[MSEL]) and the comparator output settling to a stable level.
4. 1 LSB = $V_{reference}/64$

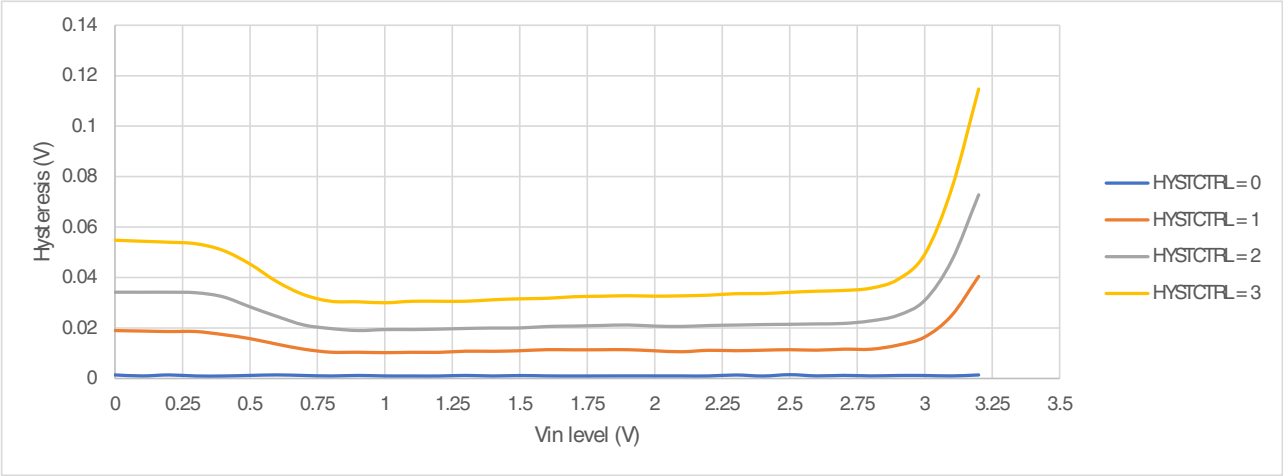


Figure 23. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 1)

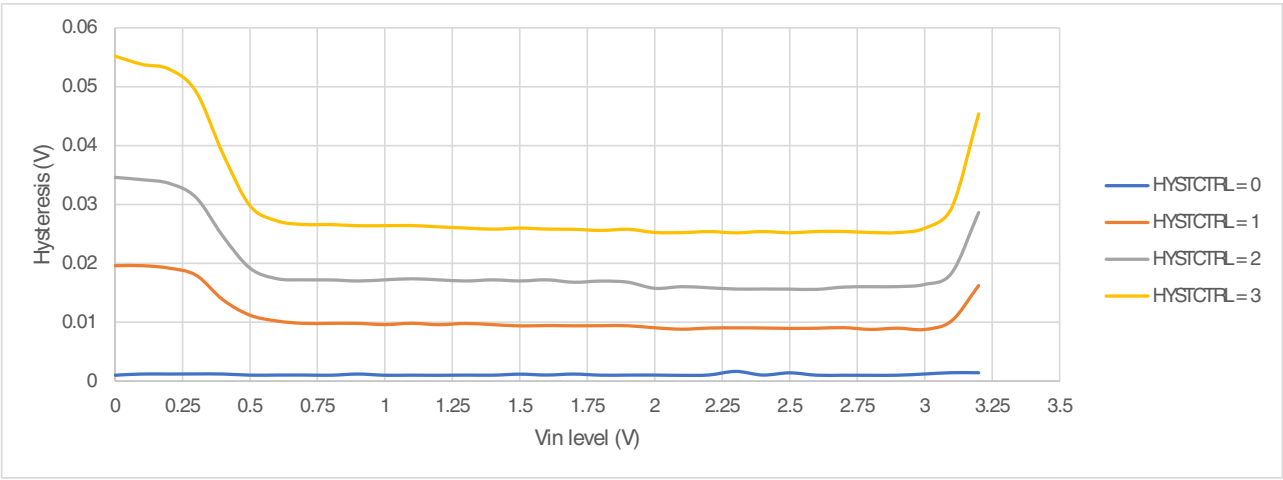


Figure 24. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 0)

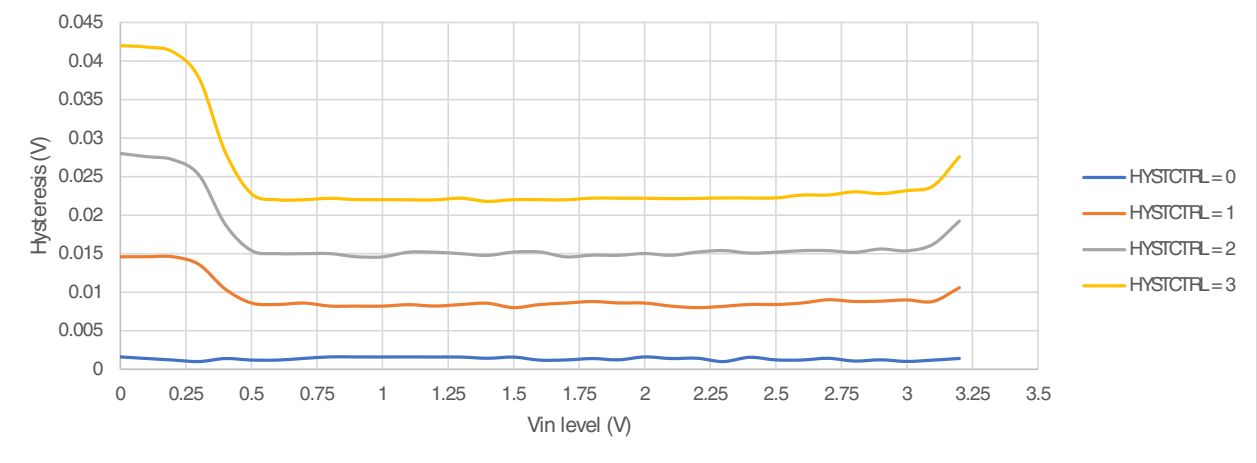


Figure 25. Typical hysteresis vs. Vin level (VDD = 3.3 V, HPMD = 0, NPMD = 1)

4.4.6.4 12-bit DAC electrical characteristics

4.4.6.4.1 12-bit DAC operating requirements

Table 98. 12-bit DAC operating requirements

Symbol	Desciption	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{DACR}	Reference voltage	1.13	3.6	V	1
C_L	Output load capacitance	—	100	pF	2
I_L	Output load current	—	1	mA	

1. The DAC reference can be selected to be V_{DDA} or V_{REF_OUT}.
2. A small load capacitance (47 pF) can improve the bandwidth performance of the DAC.

4.4.6.4.2 12-bit DAC operating behaviors

Table 99. 12-bit DAC operating behaviors

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
I_{DDA_DACLP}	Supply current — low-power mode	—	—	250	µA	
I_{DDA_DACHP}	Supply current — high-speed mode	—	—	900	µA	
t_{DACLP}	Full-scale settling time (0x080 to 0xF7F) — low-power mode	—	100	200	µs	1
t_{DACHP}	Full-scale settling time (0x080 to 0xF7F) — high-power mode	—	15	30	µs	1

Table continues on the next page...

Table 99. 12-bit DAC operating behaviors (continued)

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
$t_{CCDACLP}$	Code-to-code settling time (0xBF8 to 0xC08) — low-power mode and high-speed mode	—	0.7	1	µs	1
$V_{dacoutl}$	DAC output voltage range low — high-speed mode, no load, DAC set to 0x000	—	—	100	mV	
$V_{dacouth}$	DAC output voltage range high — high-speed mode, no load, DAC set to 0xFFF	V_{DACR} −100	—	V_{DACR}	mV	
INL	Integral non-linearity error — high speed mode	—	—	±8	LSB	2
DNL	Differential non-linearity error — V_{DACR} > 2 V	—	—	±1	LSB	3
DNL	Differential non-linearity error — V_{DACR} = VREF_OUT	—	—	±1	LSB	4
V_{OFFSET}	Offset error	—	±0.4	±0.8	%FSR	5
E_G	Gain error	—	±0.1	±0.6	%FSR	5
PSRR	Power supply rejection ratio, V_{DDA} ≥ 2.4 V	60	—	90	dB	
T_{CO}	Temperature coefficient offset voltage	—	3.7	—	µV/C	6
T_{GE}	Temperature coefficient gain error	—	0.000421	—	%FSR/C	
Rop	Output resistance (load = 3 kΩ)	—	—	250	Ω	
SR	Slew rate -80h→ F7Fh→ 80h				V/µs	
	• High power (SP_{HP})	1.2	1.7	—		
	• Low power (SP_{LP})	0.05	0.12	—		
BW	3dB bandwidth				kHz	
	• High power (SP_{HP})	550	—	—		
	• Low power (SP_{LP})	40	—	—		

1. Settling within ±1 LSB
2. The INL is measured for 0 + 100 mV to V_{DACR} −100 mV
3. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV
4. The DNL is measured for 0 + 100 mV to V_{DACR} −100 mV with V_{DDA} > 2.4 V
5. Calculated by a best fit curve from V_{SS} + 100 mV to V_{DACR} − 100 mV
6. V_{DDA} = 3.0 V, reference select set for V_{DDA} (DACx_CO:DACRFS = 1), high power mode (DACx_C0:LPEN = 0), DAC set to 0x800, temperature range is across the full range of the device

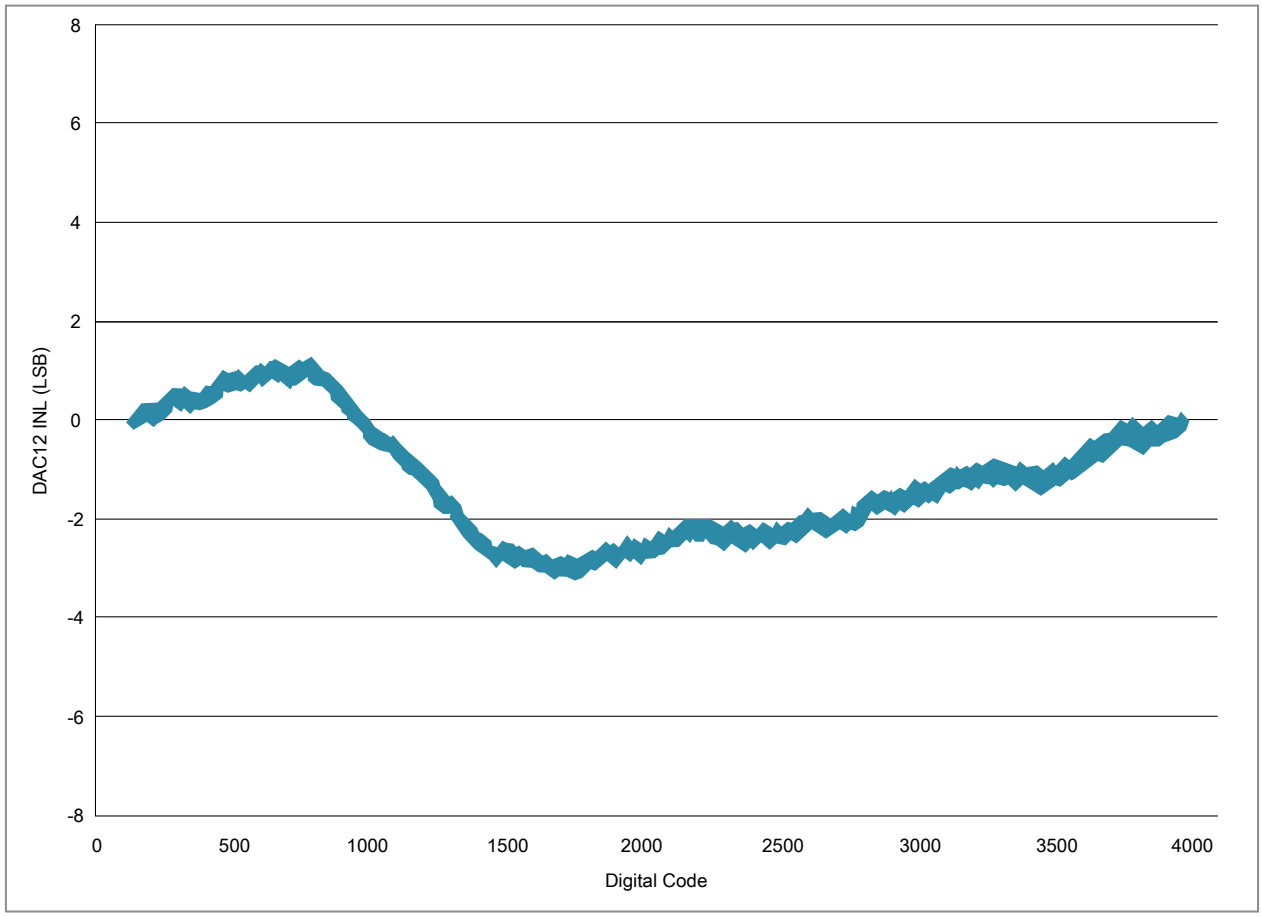


Figure 26. Typical INL error vs. digital code

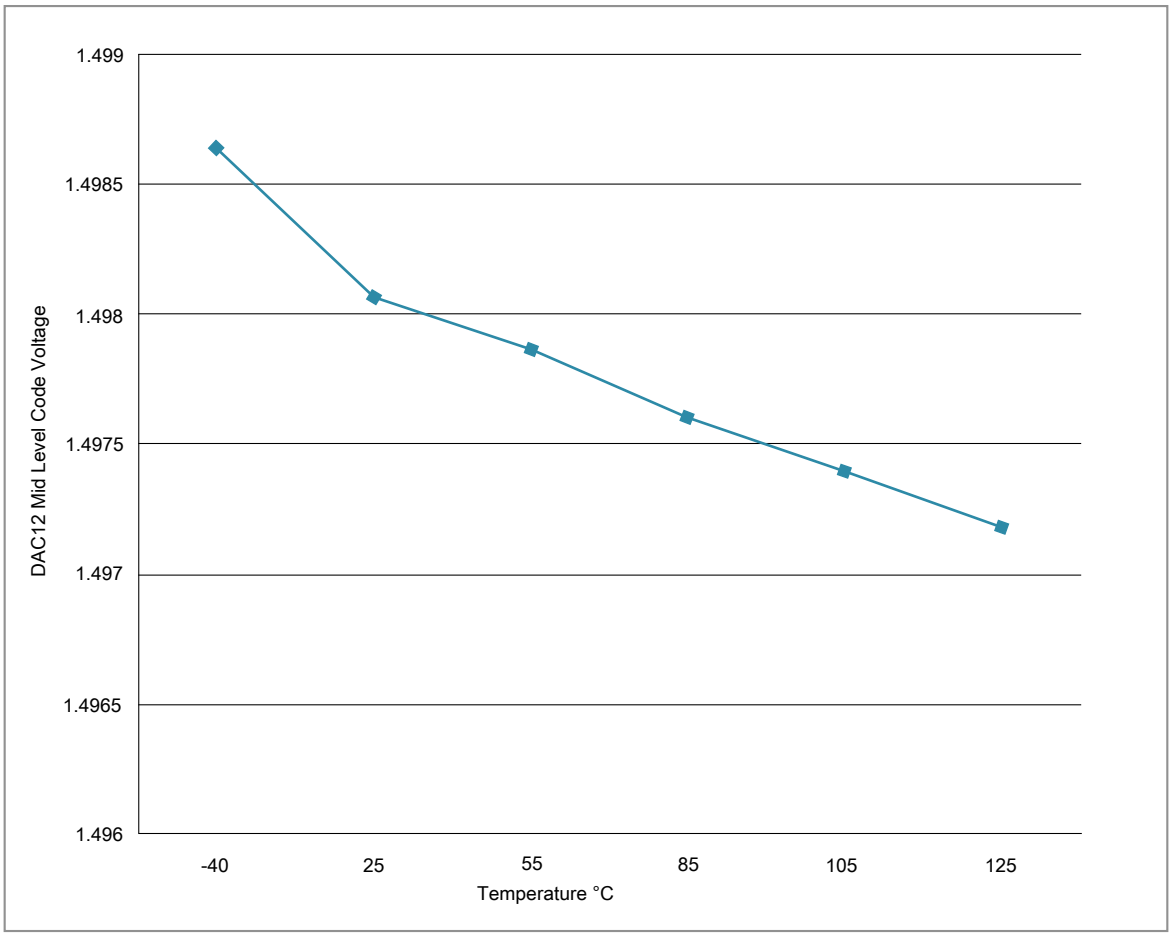


Figure 27. Offset at half scale vs. temperature

4.4.7 Timers

See General switching specifications.

4.4.8 Communication interfaces

4.4.8.1 EMV SIM specifications

Each EMV SIM module interface consists of a total of five pins.

The interface is designed to be used with synchronous Smart cards, meaning the EMV SIM module provides the clock used by the Smart card. The clock frequency is typically 372 times the Tx/Rx data rate; however, the EMV SIM module can also work with CLK frequencies of 16 times the Tx/Rx data rate.

There is no timing relationship between the clock and the data. The clock that the EMV SIM module provides to the Smart card is used by the Smart card to recover the clock from the data in the same manner as standard UART data exchanges. All five signals of the EMV SIM module are asynchronous with each other.

The smart card is initiated by the interface device; the Smart card responds with Answer to Reset. Although the EMV SIM interface has no defined requirements, the ISO/IEC 7816 defines reset and power-down sequences (for detailed information see ISO/IEC 7816).

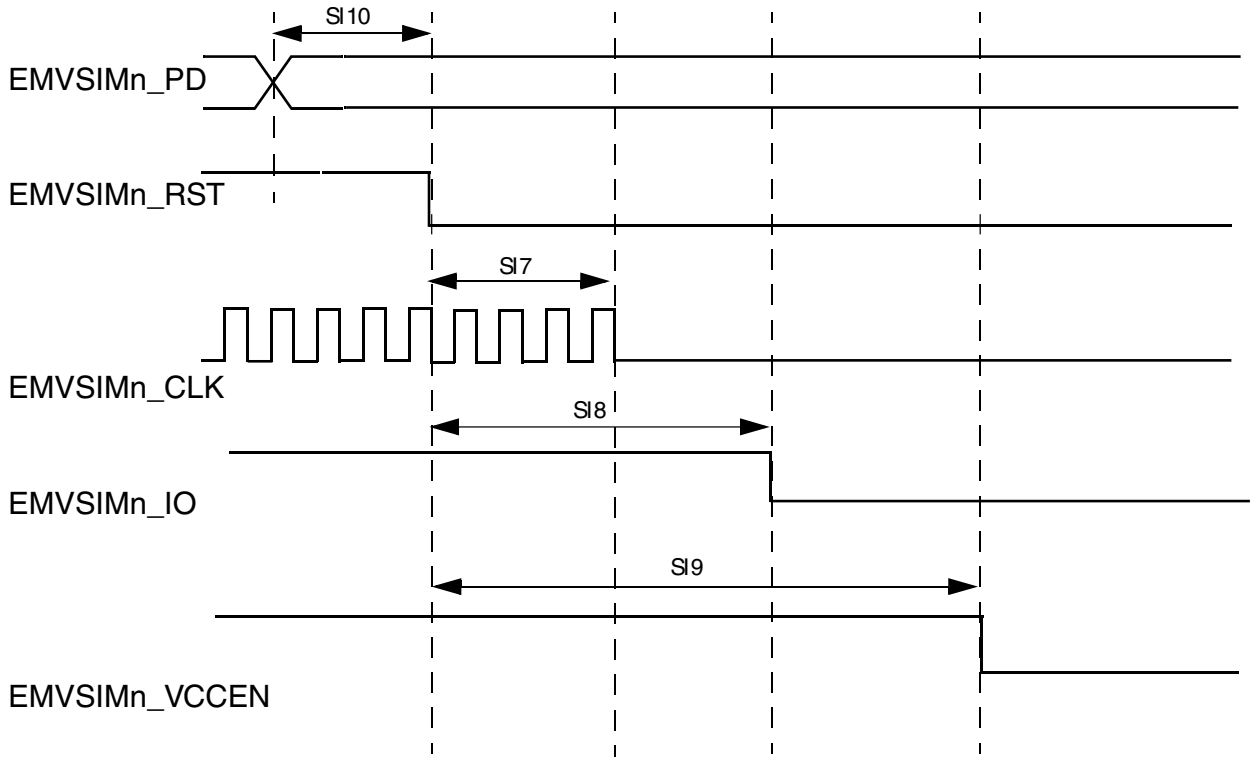


Figure 28. EMV SIM Clock Timing Diagram

The following table defines the general timing requirements for the EMV SIM interface.

Table 100. Timing Specifications, High Drive Strength

ID	Parameter	Symbol	Min	Max	Unit
SI 1	EMV SIM clock frequency (EMVSIMn_CLK)[1]	S_{freq}	1	5	MHz
SI 2	EMV SIM clock rise time (EMVSIMn_CLK)[2]	S_{rise}	—	0.08 × (1/Sfreq)	ns
SI 3	EMV SIM clock fall time (EMVSIMn_CLK)[2]	S_{fall}	—	0.08 × (1/Sfreq)	ns

Table continues on the next page...

Table 100. Timing Specifications, High Drive Strength (continued)

ID	Parameter	Symbol	Min	Max	Unit
SI 4	EMV SIM input transition time (EMVSIMn_IO, EMVSIMn_PD)	S_{tran}	20	25	ns
Si 5	EMV SIM I/O rise time / fall time (EMVSIMn_IO)[3]	Tr/Tf	—	0.8	µs
Si 6	EMV SIM RST rise time / fall time (EMVSIMn_RST)[4]	Tr/Tf	—	0.8	µs

1. 50% duty cycle clock,
2. With C = 50 pF
3. With Cin = 30 pF, Cout = 30 pF,
4. With Cin = 30 pF,

4.4.8.1.1 EMV SIM Reset Sequences

Smart cards may have internal reset, or active low reset. The following subset describes the reset sequences in these two cases.

4.4.8.1.1.1 Smart Cards with Internal Reset

Following figure shows the reset sequence for Smart cards with internal reset. The reset sequence comprises the following steps:

- After power-up, the clock signal is enabled on EMVSIMn_CLK (time T0)
- After 200 clock cycles, EMVSIMn_IO must be asserted.
- The card must send a response on EMVSIMn_IO acknowledging the reset between 400–40000 clock cycles after T0.

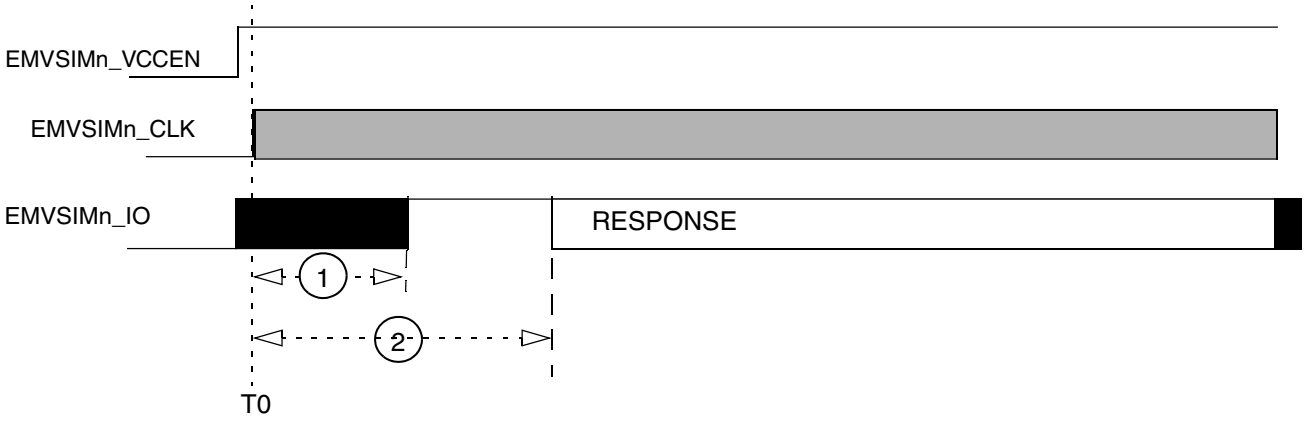


Figure 29. Internal Reset Card Reset Sequence

The following table defines the general timing requirements for the SIM interface.

Table 101. Timing Specifications, Internal Reset Card Reset Sequence

Ref	Min	Max	Units
1	—	200	EMVSIMx_CLK clock cycles
2	400	40,000	EMVSIMx_CLK clock cycles

4.4.8.1.1.2 Smart Cards with Active Low Reset

Following figure shows the reset sequence for Smart cards with active low reset. The reset sequence comprises the following steps:

- After power-up, the clock signal is enabled on EMVSIMn_CLK (time T0)
- After 200 clock cycles, EMVSIMn_IO must be asserted.
- EMVSIMn_RST must remain low for at least 40,000 clock cycles after T0 (no response is to be received on RX during those 40,000 clock cycles)
- EMVSIMn_RST is asserted (at time T1)
- EMVSIMn_RST must remain asserted for at least 40,000 clock cycles after T1, and a response must be received on EMVSIMn_IO between 400 and 40,000 clock cycles after T1.

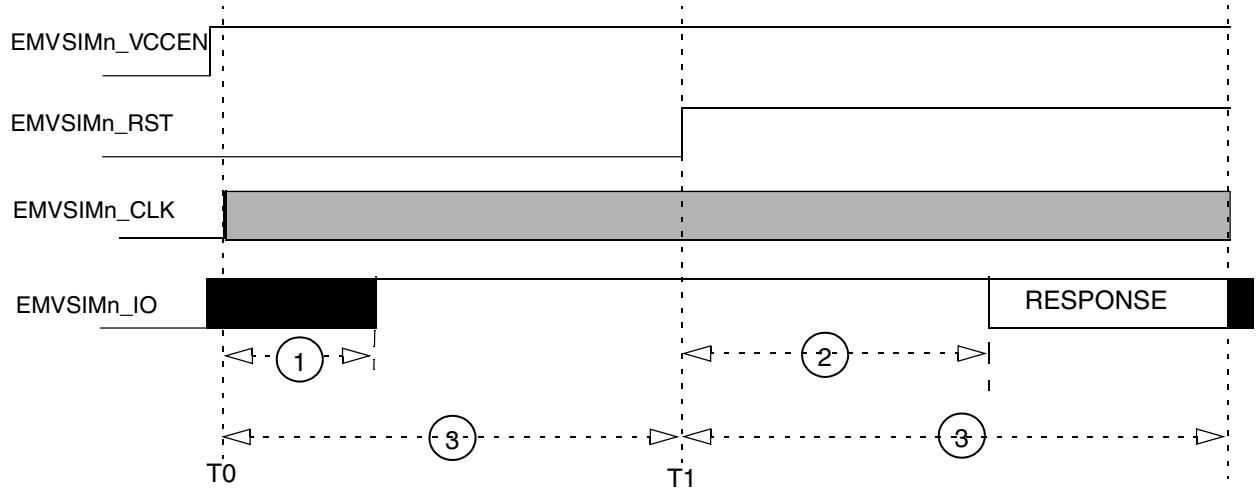


Figure 30. Active-Low-Reset Smart Card Reset Sequence

The following table defines the general timing requirements for the EMVSIM interface..

Table 102. Timing Specifications, Internal Reset Card Reset Sequence

Ref No	Min	Max	Units
1	—	200	EMVSIMx_CLK clock cycles
2	400	40,000	EMVSIMx_CLK clock cycles
3	40,000	—	EMVSIMx_CLK clock cycles

4.4.8.1.2 EMVSIM Power-Down Sequence

Following figure shows the EMV SIM interface power-down AC timing diagram.Table 103 table shows the timing requirements for parameters (SI7–SI10) shown in the figure. The power-down sequence for the EMV SIM interface is as follows:

- EMVSIMn_SIMPD port detects the removal of the Smart Card
- EMVSIMn_RST is negated
- EMVSIMn_CLK is negated
- EMVSIM_IO is negated
- EMVSIMx_VCCENy is negated

Each of the above steps requires one OSC32KCLK period (usually 32 kHz, also known as rtcclk in below figure). Power-down may be initiated by a Smart card removal detection; or it may be launched by the processor.

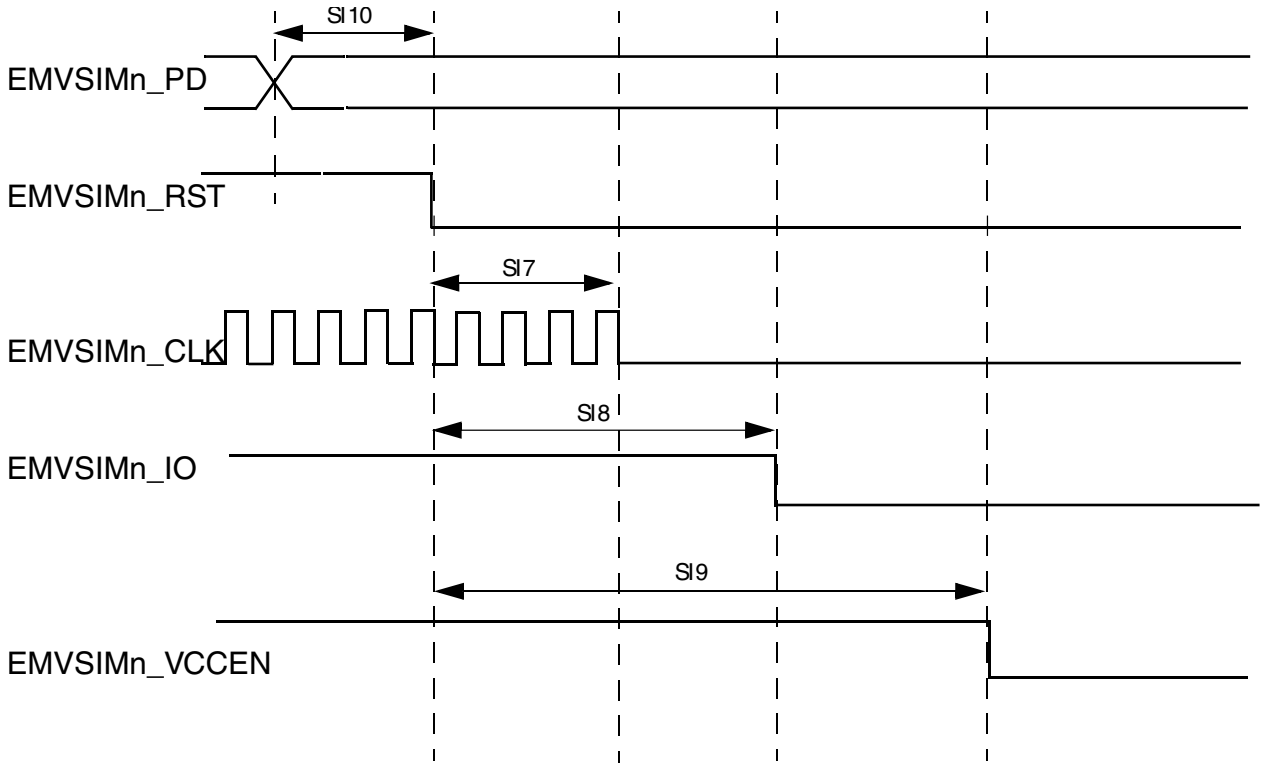


Figure 31. Smart Card Interface Power Down AC Timing

Table 103. Timing Requirements for Power-down Sequence

Ref No	Parameter	Symbol	Min	Max	Units
SI7	EMVSIM reset to SIM clock stop	$S_{rst2clk}$	0.9 × 1/ Frtcclk[1]	1.1 × 1/Frtcclk	µs
SI8	EMVSIM reset to SIM Tx data low	$S_{rst2dat}$	1.8 × 1/ Frtcclk	2.2 × 1/Frtcclk	µs
SI9	EMVSIM reset to SIM voltage enable low	$S_{rst2ven}$	2.7 × 1/ Frtcclk	3.3 × 1/Frtcclk	µs
SI10	EMVSIM presence detect to SIM reset low	S_{pd2rst}	0.9 × 1/ Frtcclk	1.1 × 1/Frtcclk	µs

1. Frtcclk is OSC32KCLK, and this clock must be enabled during the power down sequence.

NOTE

Same timing is also followed when auto power down is initiated. See Reference Manual for reference.

4.4.8.2 USB electrical specifications

The USB electricals for the USB module conform to the standards documented by the Universal Serial Bus Implementers Forum. For the most up-to-date standards, visit **usb.org**.

NOTE

The IRC48M meets the USB jitter specifications for certification in Device mode when the USB clock recovery mode is enabled. It does not meet the USB jitter specifications for certification in Host mode operation.

This device does not have the USB_CLKIN signal available and therefore cannot support Host mode operation.

4.4.8.3 USB VREG electrical specifications

Table 104. USB VREG electrical specifications

Symbol	Description	Min.	Typ.[1]	Max.	Unit	Notes
VREGIN	Input supply voltage	2.7	—	5.5	V	
I_{DDon}	Quiescent current — Run mode, load current equal zero, input supply (VREGIN) > 3.6 V	—	125	186	µA	
I_{DDstby}	Quiescent current — Standby mode, load current equal zero	—	1.1	10	µA	
I_{DDoff}	Quiescent current — Shutdown mode • VREGIN = 5.0 V and temperature=25 °C • Across operating voltage and temperature	— —	650 —	— 4	nA µA	
$I_{LOADrun}$	Maximum load current — Run mode	—	—	120	mA	
$I_{LOADstby}$	Maximum load current — Standby mode	—	—	1	mA	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) > 3.6 V • Run mode • Standby mode	 3 2.1	 3.3 2.8	 3.6 3.6	 V V	
$V_{Reg33out}$	Regulator output voltage — Input supply (VREGIN) < 3.6 V, pass-through mode	2.1	—	3.6	V	2
C_{OUT}	External output capacitor	1.76	2.2	8.16	µF	
ESR	External output capacitor equivalent series resistance	1	—	100	mΩ	
I_{LIM}	Short circuit current	—	290	—	mA	

1. Typical values assume VREGIN = 5.0 V, Temp = 25 °C unless otherwise stated.
2. Operating in pass-through mode: regulator output voltage equal to the input voltage minus a drop proportional to I_{Load}.

4.4.8.4 LPSPI switching specifications

The Low Power Serial Peripheral Interface (LPSPI) provides a synchronous serial bus with master and slave operations. Many of the transfer attributes are programmable. The following tables provide timing characteristics for classic SPI timing modes.

All timing is shown with respect to 20% V_{DD} and 80% V_{DD} thresholds, unless noted, as well as input signal transitions of 3 ns and a 30 pF maximum load on all LPSPI pins.

NOTE

- Slew rate disabled pads are those pins with PORTx_PCRn[SRE] bit cleared. Slew rate enabled pads are those pins with PORTx_PCRn[SRE] bit set.
- To achieve high bit rate, it is recommended to use fast pins (PTB[2,0], PTD[7:2], PTE[12,9:8,5:1]) and/or high drive pins (PTC[12:7], PTD[11:8], PTE[11:10]).

Table 105. LPSPI master mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—
6	t_{SU}	Data setup time (inputs)	18	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_{v}	Data valid (after SPSCK edge)	—	15	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. f_{periph} is the LPSPI peripheral functional clock.
2. $t_{periph} = 1/f_{periph}$

Table 106. LPSPI master mode timing on slew rate enabled pads

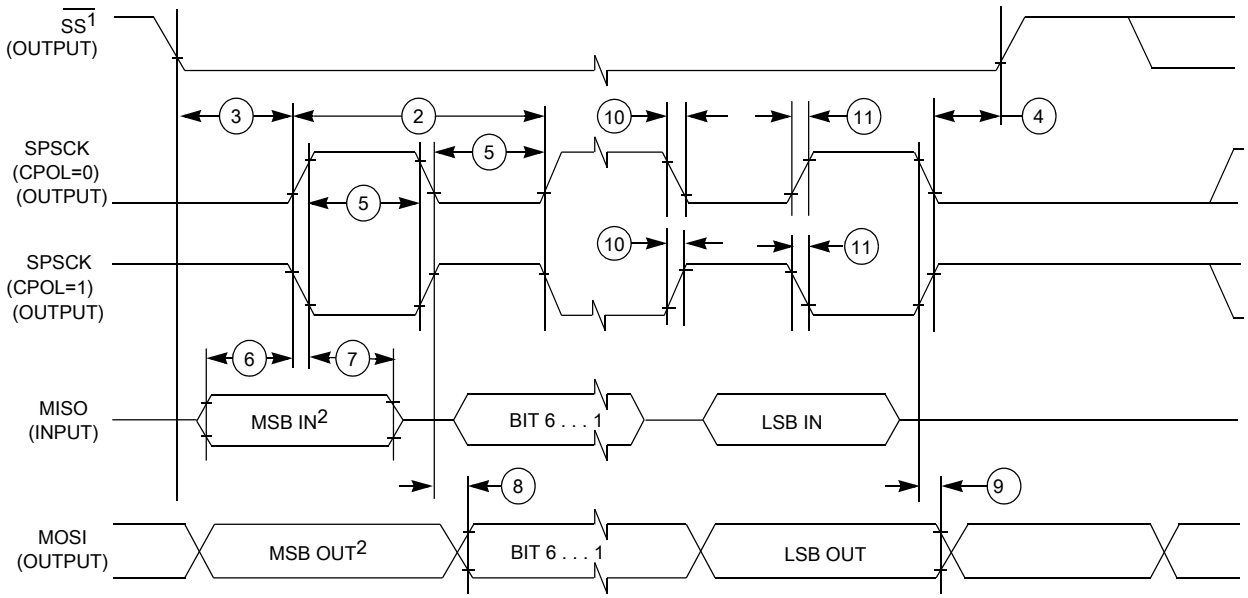
Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	$f_{periph}/2048$	$f_{periph}/2$	Hz	1
2	t_{SPSCK}	SPSCK period	2 x t_{periph}	2048 x t_{periph}	ns	2
3	t_{Lead}	Enable lead time	1/2	—	t_{SPSCK}	—
4	t_{Lag}	Enable lag time	1/2	—	t_{SPSCK}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	1024 x t_{periph}	ns	—

Table continues on the next page...

Table 106. LPSPI master mode timing on slew rate enabled pads (continued)

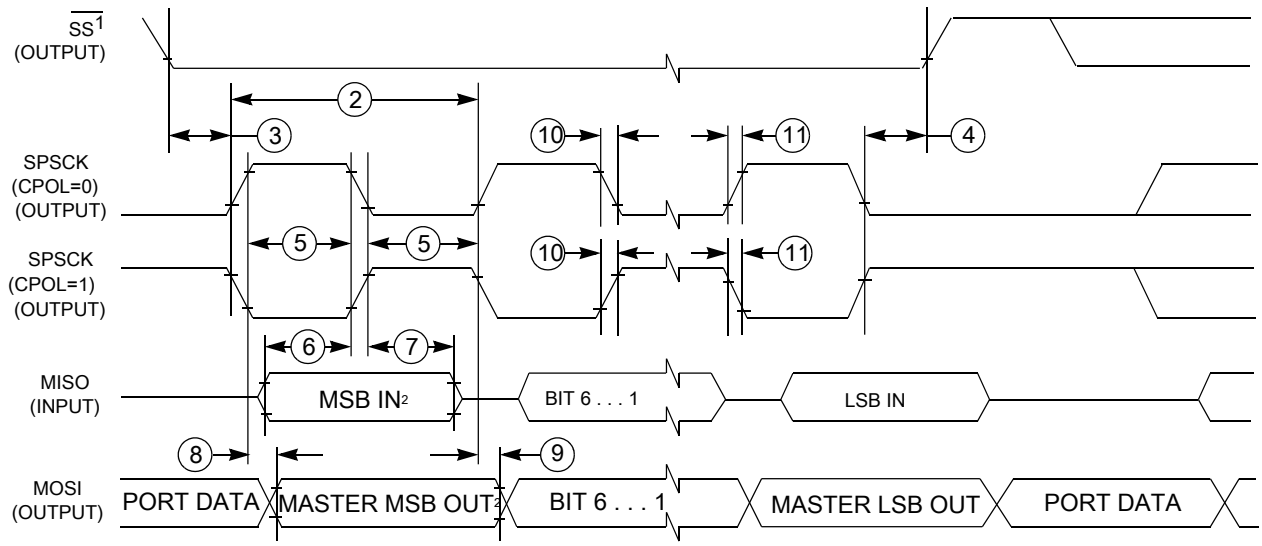
Num.	Symbol	Description	Min.	Max.	Unit	Note
6	t_{SU}	Data setup time (inputs)	96	—	ns	—
7	t_{HI}	Data hold time (inputs)	0	—	ns	—
8	t_v	Data valid (after SPSCK edge)	—	52	ns	—
9	t_{HO}	Data hold time (outputs)	0	—	ns	—
10	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
11	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. f_{periph} is the LPSPI peripheral functional clock
2. $t_{periph} = 1/f_{periph}$



1. If configured as an output.
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 32. LPSPI master mode timing (CPHA = 0)



1.If configured as output

2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 33. LPSPI master mode timing (CPHA = 1)

Table 107. LPSPI slave mode timing on slew rate disabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2.5	—	ns	—
7	t_{HI}	Data hold time (inputs)	3.5	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	31	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	25	ns	—
	t_{FO}	Fall time output				

1. f_{periph} is the LPSPI peripheral functional clock
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

Table 108. LPSPI slave mode timing on slew rate enabled pads

Num.	Symbol	Description	Min.	Max.	Unit	Note
1	f_{op}	Frequency of operation	0	$f_{periph}/4$	Hz	1
2	t_{SPSCK}	SPSCK period	4 x t_{periph}	—	ns	2
3	t_{Lead}	Enable lead time	1	—	t_{periph}	—
4	t_{Lag}	Enable lag time	1	—	t_{periph}	—
5	t_{WSPSCK}	Clock (SPSCK) high or low time	t_{periph} - 30	—	ns	—
6	t_{SU}	Data setup time (inputs)	2	—	ns	—
7	t_{HI}	Data hold time (inputs)	7	—	ns	—
8	t_a	Slave access time	—	t_{periph}	ns	3
9	t_{dis}	Slave MISO disable time	—	t_{periph}	ns	4
10	t_v	Data valid (after SPSCK edge)	—	122	ns	—
11	t_{HO}	Data hold time (outputs)	0	—	ns	—
12	t_{RI}	Rise time input	—	t_{periph} - 25	ns	—
	t_{FI}	Fall time input				
13	t_{RO}	Rise time output	—	36	ns	—
	t_{FO}	Fall time output				

1. f_{periph} is the LPSPI peripheral functional clock
2. $t_{periph} = 1/f_{periph}$
3. Time to data active from high-impedance state
4. Hold time to high-impedance state

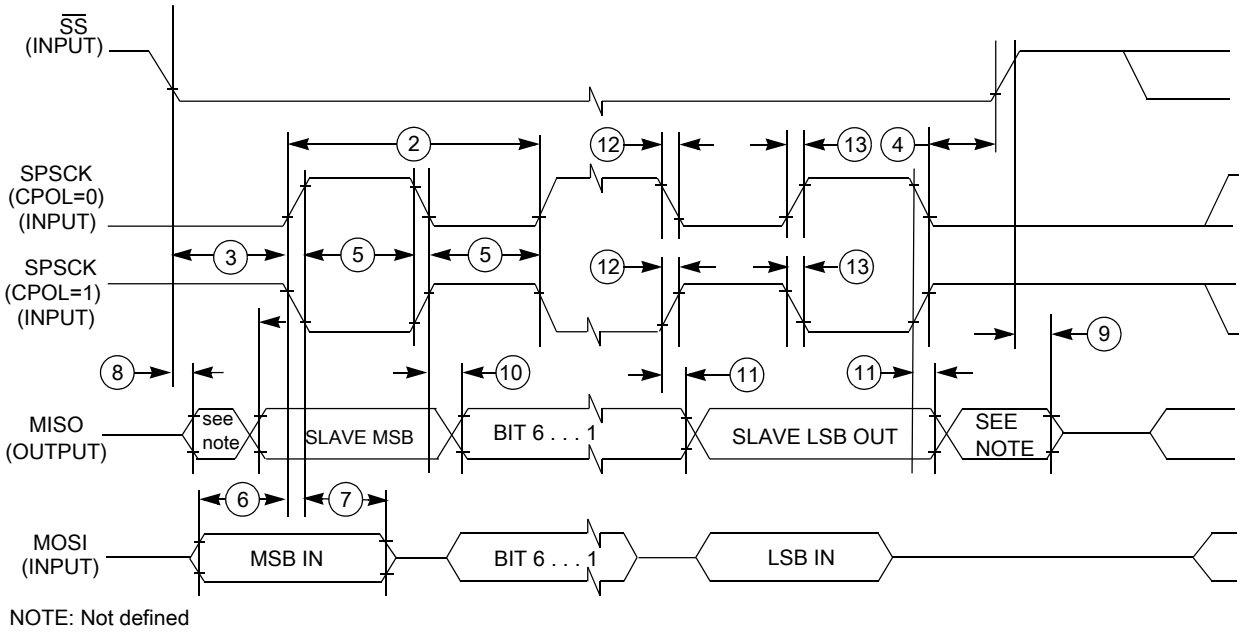


Figure 34. LPSPI slave mode timing (CPHA = 0)

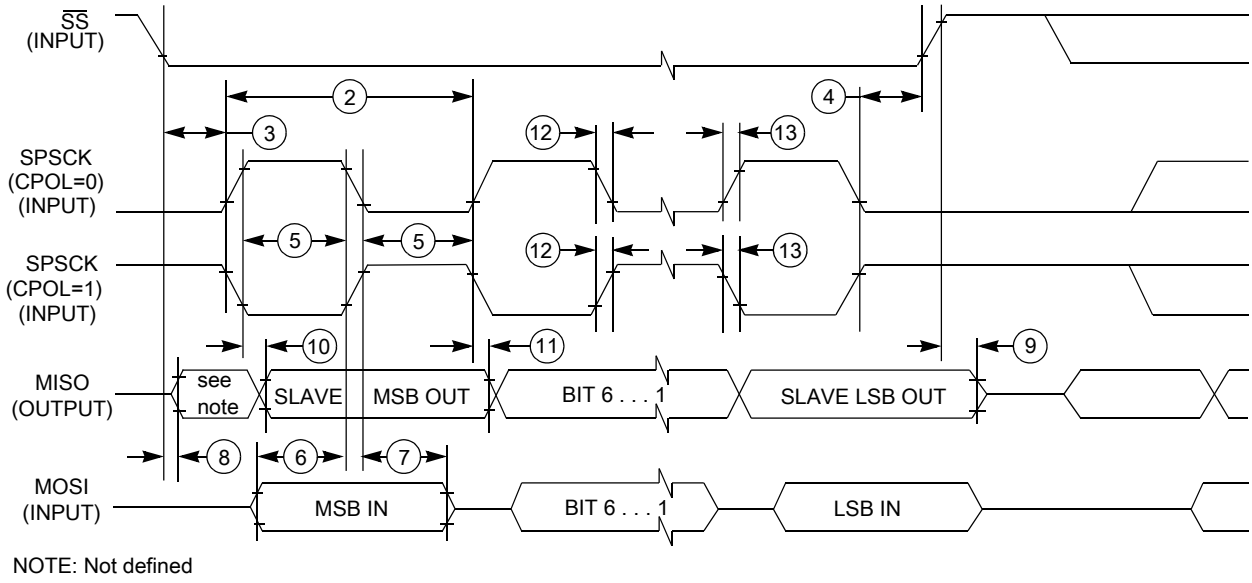


Figure 35. LPSPI slave mode timing (CPHA = 1)

4.4.8.5 LPI²C

NOTE

The LPI2C async function clock must not be faster than 24 MHz.

Table 109. LPI²C specifications

Symbol	Description		Min.	Max.	Unit	Notes
f_{SCL}	SCL clock frequency	Standard mode (Sm)	0	100	kHz	1
		Fast mode (Fm)	0	400		1, 2
		Fast mode Plus (Fm+)	0	1000		1, 3
		Ultra Fast mode (UFm)	0	5000		1, 4
		High speed mode (Hs-mode)	0	3400		1, 5

1. See General switching specifications, measured at room temperature.
2. Measured with the maximum bus loading of 400pF at 3.3V VDD with pull-up Rp = 580Ω on normal drive pins or 350Ω on high drive pins, and at 1.8V VDD with Rp = 880Ω. For all other cases, select appropriate Rp per I2C Bus Specification and the pin drive capability.
3. Fm+ is only supported on high drive pin with high drive enabled. It is measured with the maximum bus loading of 400pF at 3.3V VDD with Rp = 350Ω. For all other cases, select appropriate Rp per I2C Bus Specification and the pin drive capability.
4. UFm is only supported on high drive pin with high drive enabled and push-pull output only mode. It is measured at 3.3V VDD with the maximum bus loading of 400pF. For 1.8V VDD, the maximum speed is 4Mbps.
5. Hs-mode is only supported in slave mode and on the high drive pins with high drive enabled.

4.4.8.6 LPUART

See General switching specifications.

4.4.8.7 I2S/SAI switching specifications

This section provides the AC timing for the I2S/SAI module in master mode (clocks are driven) and slave mode (clocks are input). All timing is given for noninverted serial clock polarity (TCR2[BCP] is 0, RCR2[BCP] is 0) and a noninverted frame sync (TCR4[FSP] is 0, RCR4[FSP] is 0). If the polarity of the clock and/or the frame sync have been inverted, all the timing remains valid by inverting the bit clock signal (BCLK) and/or the frame sync (FS) signal shown in the following figures.

4.4.8.7.1 Normal Run, Wait and Stop mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in Normal Run, Wait and Stop modes.

Table 110. I2S/SAI master mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	40	—	ns
S2	I2S_MCLK (as an input) pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	80	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	15.5	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid	0	—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	19	ns
S8	I2S_TX_BCLK to I2S_TXD invalid	0	—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK	26	—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

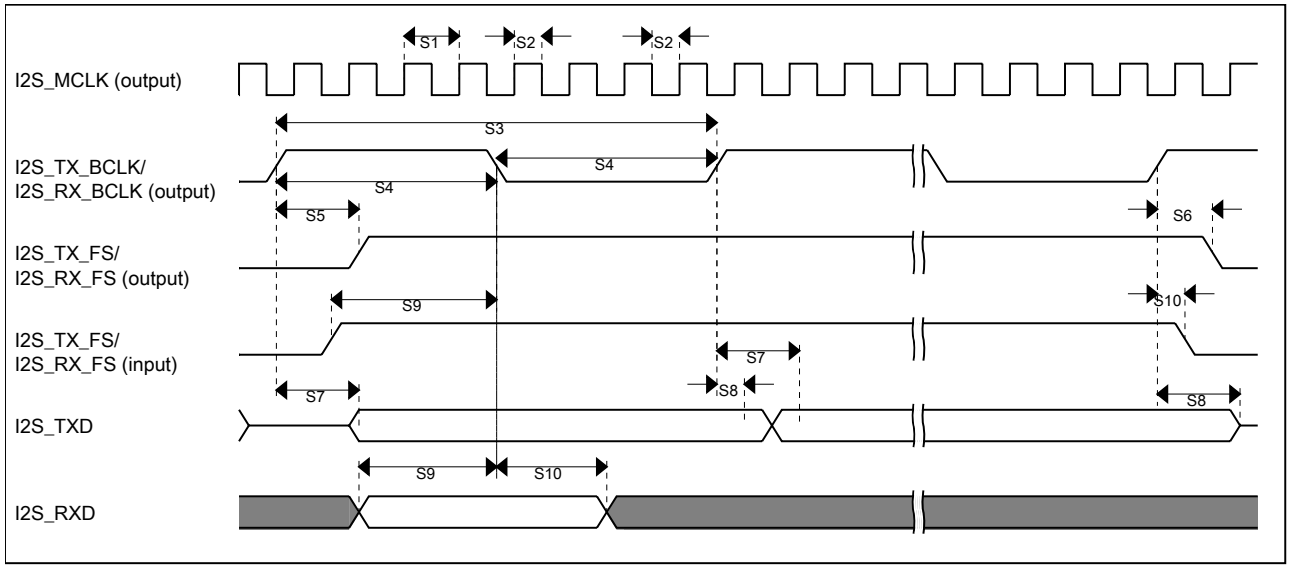


Figure 36. I2S/SAI timing — master modes

Table 111. I2S/SAI slave mode timing

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	80	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	10	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK	2	—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—	33	ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	10	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	2	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	28	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

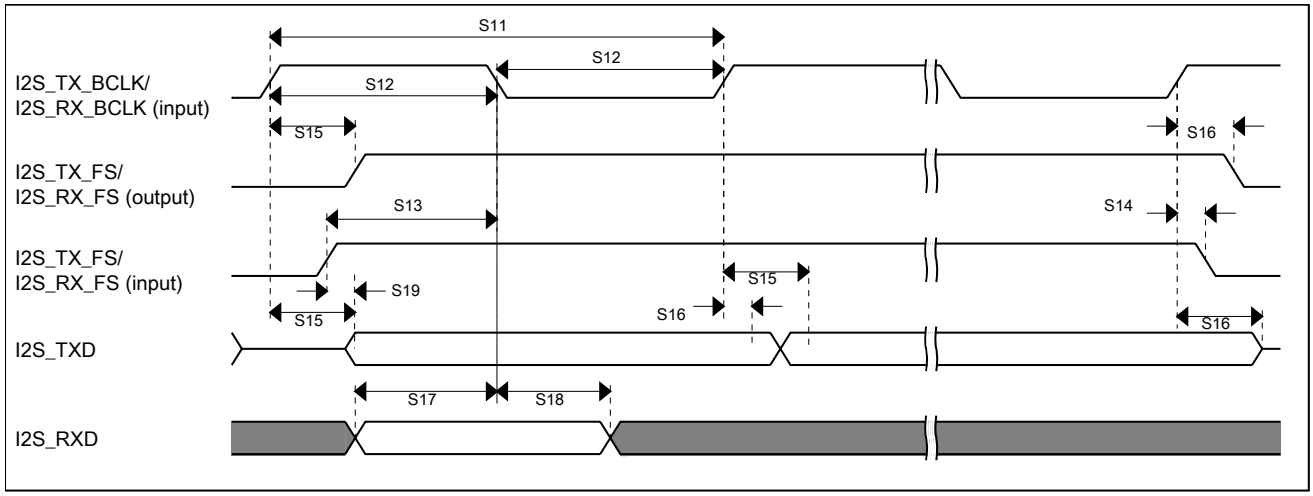


Figure 37. I2S/SAI timing — slave modes

4.4.8.7.2 VLPR, VLPW, and VLPS mode performance over the full operating voltage range

This section provides the operating performance over the full operating voltage for the device in VLPR, VLPW, and VLPS modes.

Table 112. I2S/SAI master mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S1	I2S_MCLK cycle time	62.5	—	ns
S2	I2S_MCLK pulse width high/low	45%	55%	MCLK period
S3	I2S_TX_BCLK/I2S_RX_BCLK cycle time (output)	250	—	ns
S4	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low	45%	55%	BCLK period
S5	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output valid	—	45	ns
S6	I2S_TX_BCLK/I2S_RX_BCLK to I2S_TX_FS/ I2S_RX_FS output invalid		—	ns
S7	I2S_TX_BCLK to I2S_TXD valid	—	45	ns
S8	I2S_TX_BCLK to I2S_TXD invalid		—	ns
S9	I2S_RXD/I2S_RX_FS input setup before I2S_RX_BCLK		—	ns
S10	I2S_RXD/I2S_RX_FS input hold after I2S_RX_BCLK	0	—	ns

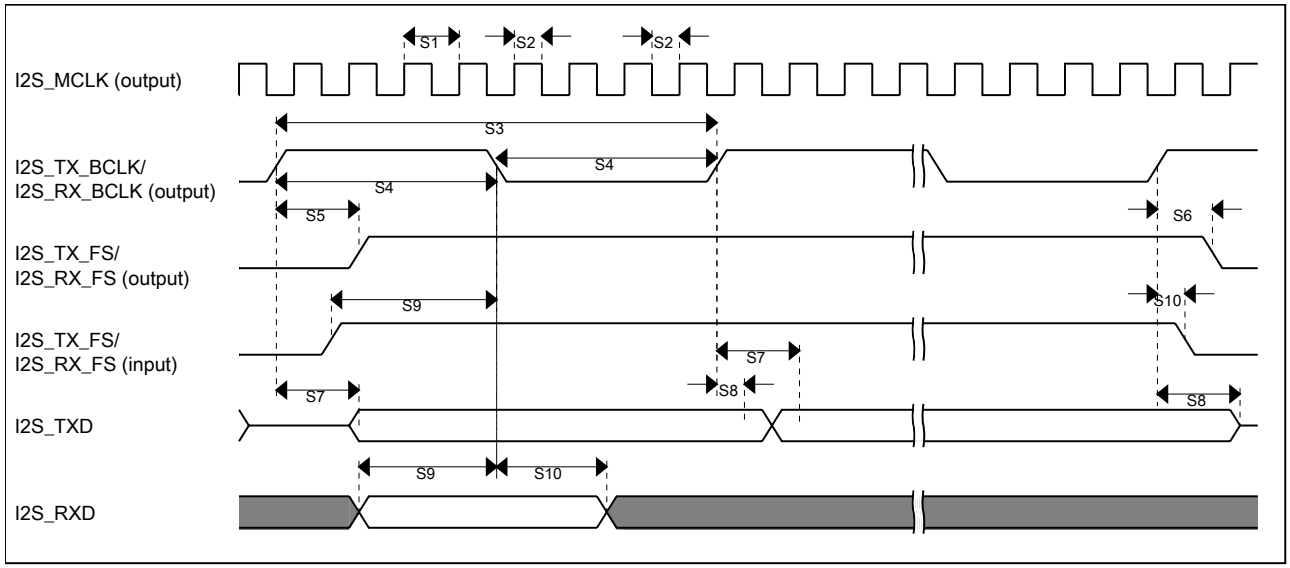


Figure 38. I2S/SAI timing — master modes

Table 113. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range)

Num.	Characteristic	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
S11	I2S_TX_BCLK/I2S_RX_BCLK cycle time (input)	250	—	ns
S12	I2S_TX_BCLK/I2S_RX_BCLK pulse width high/low (input)	45%	55%	MCLK period
S13	I2S_TX_FS/I2S_RX_FS input setup before I2S_TX_BCLK/I2S_RX_BCLK	30	—	ns
S14	I2S_TX_FS/I2S_RX_FS input hold after I2S_TX_BCLK/I2S_RX_BCLK		—	ns
S15	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output valid	—		ns
S16	I2S_TX_BCLK to I2S_TXD/I2S_TX_FS output invalid	0	—	ns
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK		—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

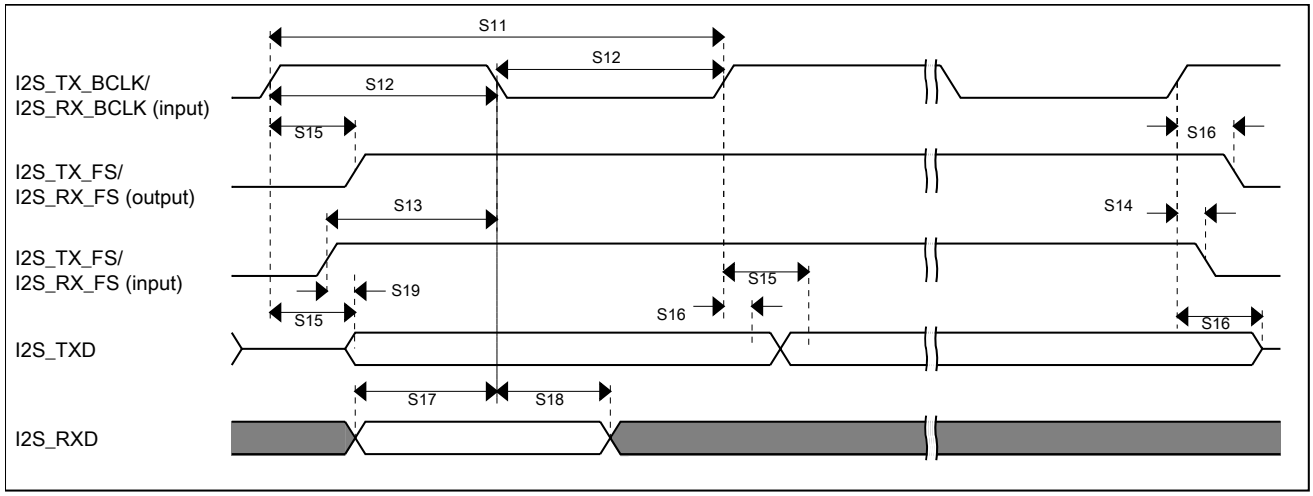


Figure 39. I2S/SAI timing — slave modes

4.4.9 DC-DC Converter Recommended Electrical Characteristics

Table 114. DC-DC Converter Recommended operating conditions

Characteristic	Symbol	Min	Typ	Max	Unit
DCDC Supply Voltage[1, 2, 3]	VDD_{DCDC_IN}	2.1	—	3.6	V
External Inductor	L_DCDC		10		µH
Inductor Resistance in Buck Mode	ESR	—	0.2	0.5	Ohms

1. The DC-DC converter generates 1.5 V at VOUT_RF and 1.225 V at VOUT_CORE pins. VOUT_RF can be used to power the VDD_RF, VDDIOx and VDDA supplies if configured to output a minimum of 1.8 V. If the system has a seperate 1.8 V supply, then it is recommended that VOUT_RF power only the VDD_RF supplies and be kept to 1.5 V.
2. The DCDC converter generates 1.225 V at VOUT_CORE. This can be used to power the VDD_CORE supplies. This supply must not be used to power any additional circuitry.
3. In Buck mode, DC-DC converter needs 2.1 V min to start, the supply can drop to 1.8 V (or VDD_RF target value + 50 mV; whichever is higher) after DC-DC converter settles.

Table 115. DC-DC Converter Specifications

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
DC-DC Converter Output Power	Total power output of VOUT_RF and VOUT_CORE	Pdcdc_out	—	—	125	mW
DC-DC Converter input voltage	—	VDCDC_IN	2.1	—	3.6	Vdc
DC-DC Converter output Voltage	—	VOUT_RF	1.500	—	2.075	Vdc
	RUN mode	VOUT_CORE	1.225	1.225	1.325	Vdc
	HSRUN mode	VOUT_CORE	1.400	1.400	1.450	Vdc
DCDC Turn on Time	—	T_{DCDC_ON}	—	5[1]	—	ms

Table continues on the next page...

Table 115. DC-DC Converter Specifications (continued)

Characteristics	Conditions	Symbol	Min	Typ	Max	Unit
VOUT_RF Output Current	—	IOUT_RF	—	—	100	mA
VOUT_CORE Output Current	—	IOUT_CORE	—	—	100	mA
Switching frequency	—	DCDC_FREQ	—	2	—	MHz
DCDC Conversion Efficiency	—	DCDC_EFF_buck	—	90%	—	
DCDC Settling Time for increasing voltage		$T_{DCDC\_SETTLE\_buck}$	—	260	—	ms/V
DCDC Settling Time for decreasing voltage		$T_{DCDC\_SETTLE\_buck}$	—	38	—	ms/V

1. Based on LDO is on and output at 1.5 V and 1.2 V. DCDC set to default 1.5 V and 1.235 V

4.4.10 Transceiver Electrical Characteristics

4.4.10.1 Recommended radio operating conditions

Table 116. Recommended operating conditions

Characteristic	Symbol	Min	Typ	Max	Unit
Bypass Mode RF and Analog Power Supply Voltage	VDD_{RF1}, VDD_{RF2}, VDD_{RF3}	1.45	1.5	3.6	Vdc
Input Frequency	fin	2.360	—	2.480	GHz
RF Input Power	Pmax	—	—	10	dBm
Crystal Reference Oscillator Frequency (±40 ppm over operating conditions to meet the 802.15.4 Standard.)	fref	26 MHz or 32 MHz			

4.4.10.2 Receiver Feature Summary

Table 117. Top level receiver specifications (T_A = 25 °C, nominal process unless otherwise noted)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Supply current power down on VDD_RFx supplies	I_{pdn}	—	200	1000	nA
Supply current Rx on with DC-DC converter enable (Buck; VDD_{DCDC_in} = 3.6 V) [3, 2]	I_{Rxon}	—	5.7	—	mA
Supply current Rx on with DC-DC converter disabled (Bypass) [2]	I_{Rxon}	—	12.8	—	mA
Input RF frequency	f_{in}	2.360	—	2.4835	GHz
GFSK Rx sensitivity(250 kb/s GFSK-BT=0.5, h=0.5)	$SENS_{GFSK}$	—	-99	—	dBm

Table continues on the next page...

Table 117. Top level receiver specifications (T_A = 25 °C, nominal process unless otherwise noted) (continued)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
GFSK Rx sensitivity(2000 kb/s GFSK-BT=0.5, h=0.5)	$SENS_{GFSK}$	—	-93	—	dBm
BLE Rx sensitivity [4]	$SENS_{BLE}$	—	-96	—	dBm
IEEE 802.15.4 Rx sensitivity [5]	$SENS_{15.4}$	—	-100	—	dBm
Noise figure for max gain mode at typical sensitivity	NF_{HG}	—	7.2	—	dB
Receiver signal strength indicator range[6]	$RSSI_{Range}$	-100	—	5	dBm
Receiver signal strength indicator resolution	$RSSI_{Res}$	—	1	—	dBm
Typical RSSI variation over frequency		-2	—	2	dB
Typical RSSI variation over temperature		-2	—	2	dB
Narrowband RSSI accuracy[7]	$RSSI_{Acc}$	-3	—	3	dB
BLE co-channel interference (Wanted signal at -67 dBm , BER <0.1%. Measurement resolution 1 MHz).	$BLE_{co\text{-}channel}$		-7		dB
IEEE 802.15.4 co-channel interference (Wanted signal 3 dB over reference sensitivity level)	$15.4_{co\text{-}channel}$	—	6	—	dB
Adjacent/Alternate Channel Performance[8]					
BLE Adjacent ±1 MHz interference offset (Wanted signal at -67 dBm , BER <0.1%. Measurement resolution 1 MHz.)	$SEL_{BLE,\ 1\ MHz}$	—	2	—	dB
BLE Adjacent ±2 MHz interference offset (Wanted signal at -67 dBm , BER <0.1%. Measurement resolution 1 MHz.)	$SEL_{BLE,\ 2\ MHz}$	—	40	—	dB
BLE Alternate ±3 MHz interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.)	$SEL_{BLE,\ 3\ MHz}$	—	50	—	dB
BLE Alternate ≥ ±4 MHz interference offset (Wanted signal at -67 dBm, BER <0.1%. Measurement resolution 1 MHz.)	$SEL_{BLE,\ 4\ MHz}$	—	55	—	dB
BLE maximum degradation with BLE carrier offset (CFO) between ± 150 kHz (25 kHz step)	CFO_{BLE}	—	3	—	dB
IEEE 802.15.4 Adjacent ±5 MHz interference offset (Wanted signal 3 dB over reference sensitivity level , PER <1%)	$SEL_{15.4,5\ MHz}$	—	55	—	dB
IEEE 802.15.4 Alternate ≥ ±10 MHz interference offset (Wanted signal 3 dB over reference sensitivity level , PER <1%.)	$SEL_{15.4,5\ MHz}$	—	60	—	dB
Intermodulation Performance					
BLE intermodulation with continuous wave interferer at ±3 MHz and modulated interferer is at ±6 MHz (Wanted signal at -67 dBm , BER<0.1%.)		—	-24	—	dBm
BLE intermodulation with continuous wave interferer at ±5 MHz and modulated interferer is at ±10 MHz (Wanted signal at -67 dBm , BER<0.1%.)		—	-35	—	dBm
Blocking Performance[8]					

Table continues on the next page...

Table 117. Top level receiver specifications (T_A = 25 °C, nominal process unless otherwise noted) (continued)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
BLE out of band blocking from 30 MHz to 1000 MHz and 4000 MHz to 5000 MHz (Wanted signal at -67 dBm , BER<0.1%. Interferer continuous wave signal.)[9]	—	—	10	—	dBm
BLE out of band blocking from 1000 MHz to 2000 MHz and 3000 MHz to 4000MHz (Wanted signal at -67 dBm , BER<0.1%. Interferer continuous wave signal.)	—	—	8	—	dBm
BLE out of band blocking from 2001 MHz to 2339 MHz and 2484 MHz to 2999 MHz (Wanted signal at -67 dBm , BER<0.1%. Interferer continuous wave signal.)	—	—	0	—	dBm
BLE out of band blocking from 5000 MHz to 12750 MHz (Wanted signal at -67 dBm , BER<0.1%. Interferer continuous wave signal.)[9]	—	—	10	—	dBm
BLE out of band blocking from 2300 MHz to 2400 MHz (LTE Band40) (Wanted signal at -67 dBm , BER<0.1%. Interferer continuous wave signal.)	—	—	-4	—	dBm
BLE out of band blocking from 2496 MHz to 2690 MHz (LTE Band41) (Wanted signal at -67 dBm ,BER<0.1%. Interferer continuous wave signal.)	—	—	0	—	dBm
IEEE 802.15.4 out of band blocking for frequency offsets > 10 MHz and <= 80 MHz(Wanted signal 3 dB over reference sensitivity level , PER <1%. Interferer continuous wave signal.)[10]		—	-20	—	dBm
IEEE 802.15.4 out of band blocking from carrier frequencies in 1 GHz to 4 GHz range excluding frequency offsets < ±80 MHz (Wanted signal 3 dB over reference sensitivity level , PER <1%. Interferer continuous wave signal.)		—	-10	—	dBm
IEEE 802.15.4 out of band blocking frequency from carrier frequencies < 1 GHz and > 4 GHz (Wanted signal 3 dB over reference sensitivity level , PER <1%. Interferer continuous wave signal.[9]		—	-2	—	dBm
Spurious Emission < 1.6 MHz offset (Measured with 100 kHz resolution and average detector. Device transmit on RF channel with center frequency fc and spurious power measured in 1 MHz at RF frequency f), where |f-fc|< 1.6 MHz	—	—	-54	—	dBc
Spurious Emission > 2.5 MHz offset (Measured with 100 kHz resolution and average detector. Device transmit on RF channel with center frequency fc and spurious power measured in 1 MHz at RF frequency f), where |f-fc|> 2.5 MHz[11]	—	—	-70	—	dBc

1. All the RX parameters are measured at the RF pins
2. Transceiver power consumption
3. DCDC default target values are used. RF supply voltage is set to 1.5V.
4. Measured at 0.1% BER using 37 byte long packets in max gain mode and nominal conditions
5. In max gain mode and nominal conditions
6. RSSI performance in narrowband mode
7. With one point calibration over frequency and temperature

8. BLE Adjacent and Block parameters are measured with modulated interference signals
9. Exceptions allowed for carrier frequency harmonics.
10. Exception to the 10 MHz > freq offset <= 80 MHz out-of-band blocking limit allowed for frequency offsets of twice the reference frequency(fref).
11. Exceptions allowed for twice the reference clock frequency(fref) multiples.

Table 118. Receiver specifications with generic FSK modulations

				Adjacent/Alternate channel selectivity (dB)[1]					
Modulation type	**Data rate (kb/s)**	**Channel BW (kHz)**	**Typical sensitivity (dBm)**	**Desired signal level (dBm)**	**Interferer at ±1* channel BW offset**	**Interferer at ±2* channel BW offset**	**Interferer at ±3* channel BW offset**	**Interferer at ±4* channel BW offset**	**Co-channel**
GFSK BT = 0.5, h = 0.5	2000	4000	-93	-67	45	50	55	58	-5
	1000	2000	-95.5	-67	45	55	55	50	-8
	500	1000	-98	-85	40	50	55	55	-6
	250	500	-99	-85	27	38	44	48	-6
GFSK, BT = 0.5, h = 0.3	2000	2000	-88	-67	37	45	47	47	-12
	1000	1000	-91	-67	35	45	40	49	-14
	500	800	-93.4	-85	22	30	37	41	-11
	250	500	-94.6	-85	19	25	30	34	-10
GFSK, BT = 0.5, h = 0.7	1000	2000	-96.5	-85	42	50	53	55	-8
	500	1000	-98.6	-85	40	50	55	55	-6
	250	600	-99.2	-85	28.7	38	46	50	-7
GMSK BT = 0.3	2000	3200	-88.5	-80	37	40	47	50	-10
	1000	1600	-92.4	-85	37	44	45	50	-7.2
	500	800	-94.3	-85	22	30	36	41	-7
	250	500	-95.8	-85	18	25	30	34	-6
GMSK, BT = 0.7	2000	4000	-93.9	-85	43	52	55	57	-8
	1000	2000	-96.8	-85	40	50	52	55	-7
	500	1000	-98.5	-85	40	50	55	55	-6
	250	600	-99.3	-85	30	40	46	50	-7
Generic MSK	2000	6000	-94.5	-85	35	45	55	57	-9
	1000	3000	-96.9	-85	23	30	40	45	-7
	500	1600	-98.7	-85	32	42	49	55	-6
	250	800	-100	-85	26	34	40	46	-5
GFSK, BT = 0.5, h = 1.0	1000	1600	-94.5	-85	45	52	57	60	-11.5
	500	800	-96.8	-85	26	36	42	47	-10
	250	400	-96.8	-85	20	29	35	40	-10

1. Selectivity measured with an unmodulated blocker

4.4.10.3 Transmit and PLL Feature Summary

- Supports constant envelope modulation of 2.4 GHz ISM and 2.36 GHz MBAN frequency bands
- Fast PLL Lock time: < 25 µs
- Reference Frequency:
  - 26 and 32 MHz supported for BLE and FSK modes
  - 32 MHz supported for IEEE Standard 802.15.4

Table 119. Top level Transmitter Specifications (TA=25°C, nominal process unless otherwise noted)

Characteristic[1]	Symbol	Min.	Typ.	Max.	Unit
Supply current power down on VDD_RFx supplies	I_{pdn}	—	200	—	nA
Supply current Tx On with P_{RF} = 0dBm and DC-DC converter enabled (Buck; VDD_{DCDC_in} = 3.6 V) [2]	I_{Txone}	—	5.7	—	mA
Supply current Tx On with P_{RF} = 0 dBm and DC-DC converter disabled (Bypass) [2]	I_{Txond}	—	12.7	—	mA
Output Frequency	f_c	2.360	—	2.4835	GHz
Maximum RF Output power [3]	$P_{RF,max}$	—	3.5	—	dBm
Minimum RF Output power [3]	$P_{RF,min}$	—	-30	—	dBm
RF Output power control range	P_{RFCR}	—	34	—	dB
IEEE 802.15.4 Peak Frequency Deviation	$F_{dev15.4}$	—	±500	—	kHz
IEEE 802.15.4 Error Vector Magnitude[4]	$EVM_{15.4}$		4	8	%
IEEE 802.15.4 Offset Error Vector Magnitude[5]	$OEVM_{15.4}$		0.5	2	%
IEEE 802.15.4 TX spectrum level at 3.5MHz offset[4, 6]	$TXPSD_{15.4}$			-40	dBc
BLE TX Output Spectrum 20dB BW	$TXBW_{BLE}$	1.0		—	MHz
BLE average frequency deviation using a 00001111 modulation sequence	$\Delta f1_{avg,BLE}$		250		kHz
BLE average frequency deviation using a 01010101 modulation sequence	$\Delta f2_{avg,BLE}$		220		kHz
BLE RMS FSK Error	$FSK_{err,BLE}$		3%		
BLE Maximum Deviation of the Center Frequency[7]	$F_{cdev,BLE}$	—	±10	—	kHz
BLE Adjacent Channel Transmit Power at 2MHz offset[6]	$P_{RF2MHz,BLE}$	—	—	-50	dBm
BLE Adjacent Channel Transmit Power at >= 3MHz offset[6]	$P_{RF3MHz,BLE}$	—	—	-55	dBm
BLE in-band spectral emissions at fc ±4 MHz offset (adjacent channel transmitt power)	$P_{RF4MHz,BLE}$	—	—	-60	dBm
BLE Frequency Hopping Support			YES		
2nd Harmonic of Transmit Carrier Frequency (Pout = PRF,max)[8]	TXH2	—	-46	—	dBm/MHz
3rd Harmonic of Transmit Carrier Frequency (Pout = PRF,max)[8]	TXH3	—	-58	—	dBm/MHz

1. All the TX parameters are measured at test hardware SMA connector
2. Transceiver power consumption

3. Measured at the RF pins
4. Measured as per IEEE Standard 802.15.4
5. Offset EVM is computed at one point per symbol, by combining the I value from the beginning of each symbol and the Q value from the middle of each symbol into a single complex value for EVM computations
6. Measured at $P_{RF,max}$ and recommended TX match
7. Maximum drift of carrier frequency of the PLL during a BLE packet with a nominal 32MHz reference crystal
8. Harmonic Levels based on recommended 2 component match. Transmit harmonic levels depend on the tolerances and quality of the matching components.

Transmit PA driver output as a function of the PA_POWER[5:0] field when measured at the IC pins is as follows:

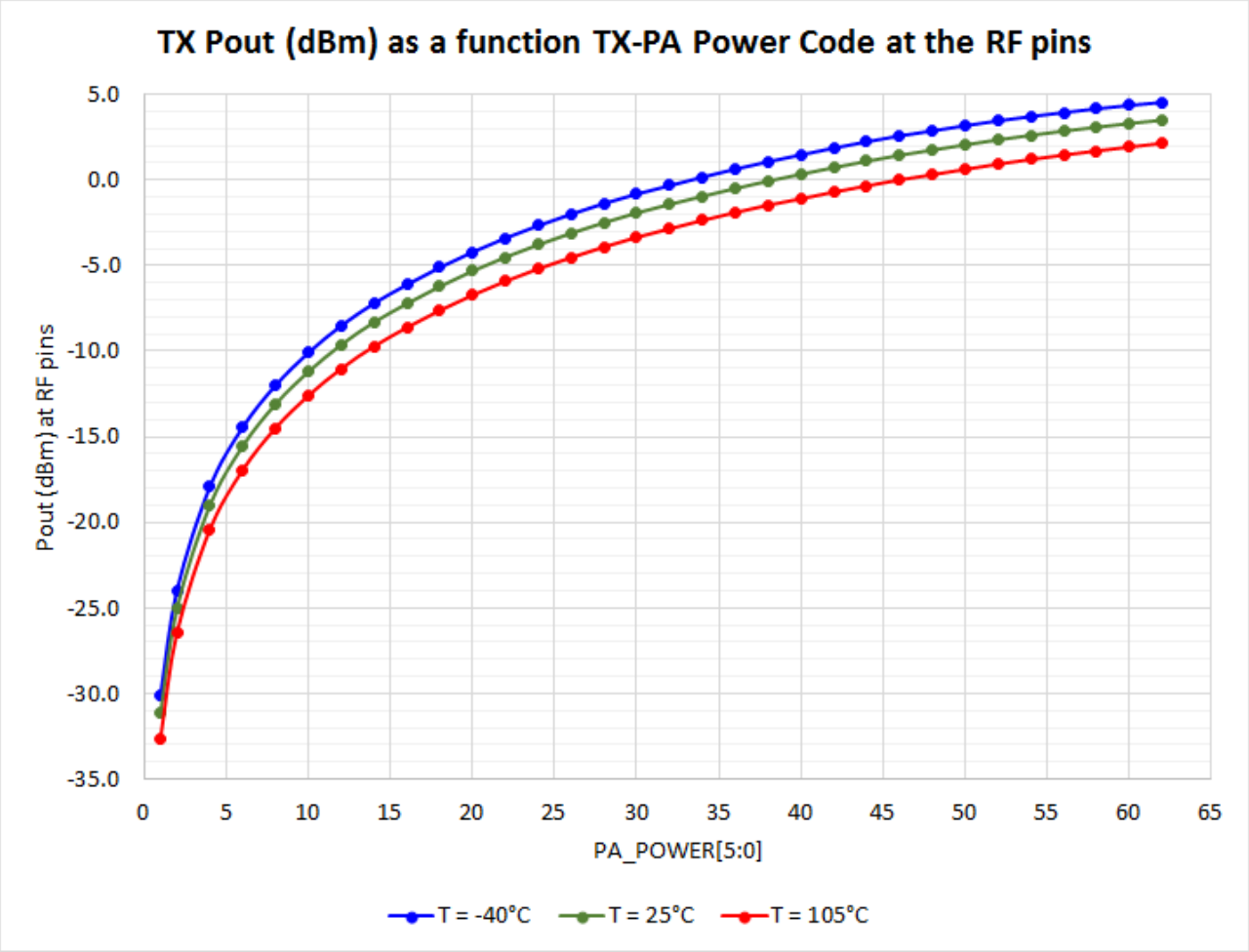


Table 120. Transmit Output Power as a function of PA_POWER[5:0]

	TX Pout (dBm)		
PA_POWER[5:0]	T = -40 °C	T = 25 °C	T = 105 °C
1	-30.1	-31.1	-32.6
2	-24.0	-25.0	-26.4
4	-17.9	-19.0	-20.4
6	-14.5	-15.6	-17.0
8	-12.0	-13.1	-14.5
10	-10.1	-11.2	-12.6
12	-8.5	-9.6	-11.0
14	-7.2	-8.3	-9.7
16	-6.1	-7.2	-8.6
18	-5.1	-6.2	-7.6
20	-4.2	-5.3	-6.7
22	-3.4	-4.5	-5.9
24	-2.7	-3.8	-5.2
26	-2.0	-3.1	-4.5
28	-1.4	-2.5	-3.9
30	-0.8	-1.9	-3.3
32	-0.3	-1.4	-2.8
34	0.2	-1.0	-2.4
36	0.6	-0.5	-1.9
38	1.1	-0.1	-1.5
40	1.5	0.3	-1.1
42	1.9	0.7	-0.7
44	2.2	1.1	-0.3
46	2.6	1.4	0.0
48	2.9	1.8	0.3
50	3.2	2.1	0.6
52	3.5	2.4	0.9
54	3.7	2.6	1.2
56	3.9	2.9	1.5
58	4.2	3.1	1.7
60	4.4	3.3	1.9
62	4.5	3.5	2.1

5 Design considerations

5.1 Hardware design considerations

This device contains protective circuitry to guard against damage due to high static voltage or electric fields. However, take normal precautions to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit.

5.1.1 Printed circuit board recommendations

- Place connectors or cables on one edge of the board and do not place digital circuits between connectors.
- Drivers and filters for I/O functions must be placed as close to the connectors as possible. Connect TVS devices at the connector to a good ground. Connect filter capacitors at the connector to a good ground.
- Physically isolate analog circuits from digital circuits if possible.
- Place input filter capacitors as close to the MCU as possible.
- For best EMC performance, route signals as transmission lines; use a ground plane directly under LQFP packages; and solder the exposed pad (EP) to ground directly under QFN packages.

5.1.2 Power delivery system

Consider the following items in the power delivery system:

- Use a plane for ground.
- Use a plane for MCU VDDIOx supply if possible.
- Always route ground first, as a plane or continuous surface, and never as sequential segments.
- Route power next, as a plane or traces that are parallel to ground traces.
- Place bulk capacitance, 10 µF or more, at the entrance of the power plane.
- Place bypass capacitors for MCU power domain as close as possible to each VDDIOx/VSS pair, including VDDA/VSSA and VREFH/VREFL.
- The minimum bypass requirement is to place 0.1 µF capacitors positioned as near as possible to the package supply pins.
- It is recommended to include a filter circuit with one bulk capacitor (no less than 2.2 µF) and one 0.1 µF capacitor at the VREGIN and VOUT33 pins to improve USB performance.
- Take special care to minimize noise levels on the VREFH/VREFL inputs. An option is to use the internal reference voltage (output 1.2 V/2.1 V typically) as the ADC reference.

- VDDIO2 is dedicated to powering PORTE.
- VDDA must be higher or equal to VDDIO1 and VDDIO2.

5.1.3 Analog design

Each ADC input must have an RC filter as shown in the following figure. The maximum value of R must be RAS max if fast sampling and high resolution are required. The value of C must be chosen to ensure that the RC time constant is very small compared to the sample period.

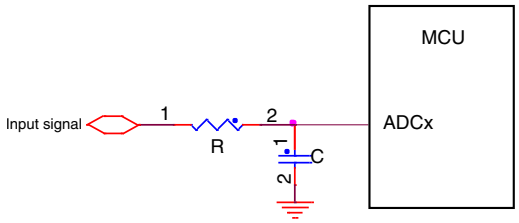


Figure 40. RC circuit for ADC input

High voltage measurement circuits require voltage division, current limiting, and over-voltage protection as shown the following figure. The voltage divider formed by R1 – R4 must yield a voltage less than or equal to VREFH. The current must be limited to less than the injection current limit. Since the ADC pins do not have diodes to VDD, external clamp diodes must be included to protect against transient over-voltages.

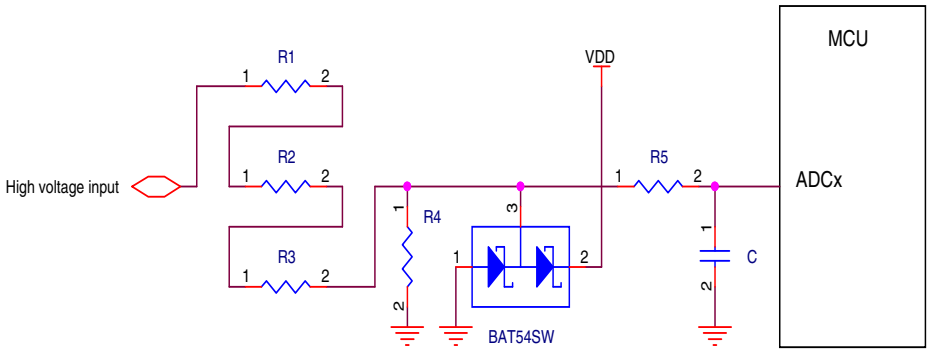


Figure 41. High voltage measurement with an ADC input

5.1.4 Digital design

Ensure that all I/O pins cannot get pulled above VDDIOx (Max I/O is VDDIOx+0.3V).

CAUTION

Do not provide power to I/O pins prior to VDDIOx, especially the RESET_b pin.

- RESET_b pin

  The RESET_b pin is an open-drain I/O pin that has an internal pullup resistor. An external RC circuit is recommended to filter noise as shown in the following figure. The resistor value must be in the range of 4.7 kΩ to 10 kΩ; the recommended capacitance value is 0.1 µF. The RESET_b pin also has a selectable digital filter to reject spurious noise.

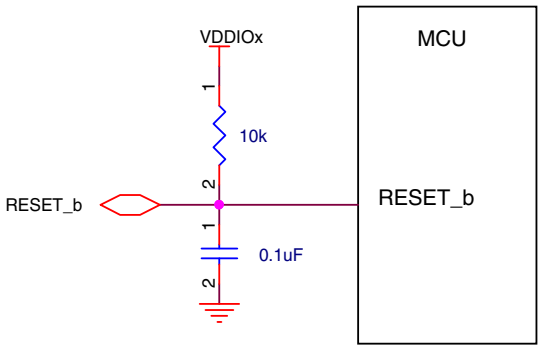


Figure 42. Reset circuit

When an external supervisor chip is connected to the RESET_b pin, a series resistor must be used to avoid damaging the supervisor chip or the RESET_b pin, as shown in the following figure. The series resistor value (RS below) must be in the range of 100 Ω to 1 kΩ depending on the external reset chip drive strength. Select the open-drain output from the supervisor chip.

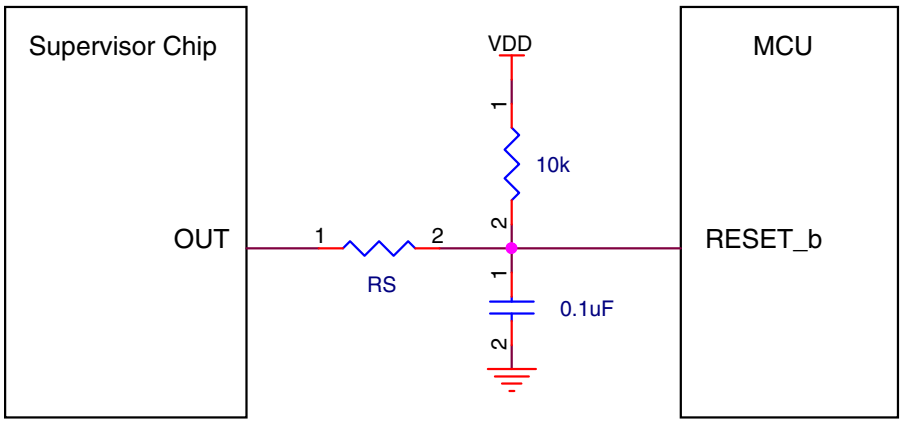


Figure 43. Reset signal connection to external reset chip

- NMI pin

  Do not add a pull-down resistor or capacitor on the NMI_b pin, because a low level on this pin will trigger non-maskable interrupt. When this pin is enabled as the NMI function, an external pull-up resistor (10 kΩ) as shown in the following figure is recommended for robustness.

  If the NMI_b pin is used as an I/O pin, the non-maskable interrupt handler is required to disable the NMI function by remapping to another function. The NMI function is disabled by programming the FOPT[NMI_DIS] bit to zero.

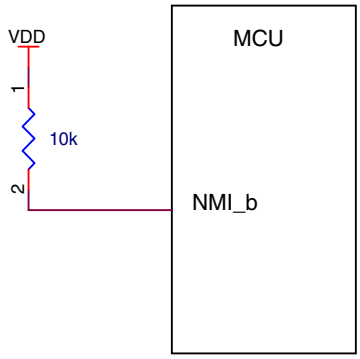


Figure 44. NMI pin biasing

- Debug interface

  This MCU uses the standard ARM SWD and JTAG interface protocol as shown in the following figure. While pull-up or pull-down resistors are not required (SWD_DIO has an internal pull-up and SWD_CLK has an internal pull-down), external 10 kΩ pull resistors are recommended for system robustness. The RESET_b pin recommendations mentioned above must also be considered.

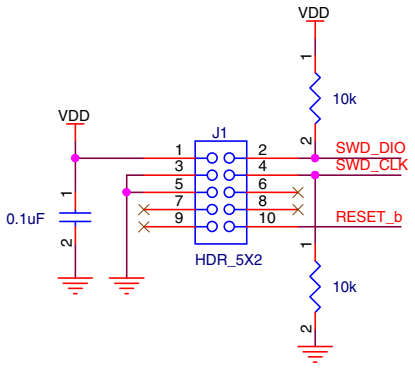


Figure 45. SWD debug interface

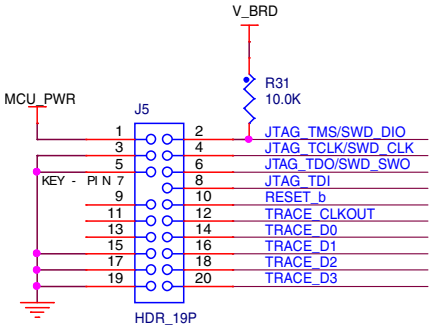


Figure 46. JTAG debug interface

- Low leakage stop mode wakeup

  Select low leakage wakeup pins (LLWU_Px) to wake the MCU from one of the low leakage stop modes (LLS/VLLSx). See RV32M1 subfamily Pinout for pin selection.

- Unused pin

  Unused GPIO pins must be left floating (no electrical connections) with the MUX field of the pin's PORTx_PCRn register equal to 0:0:0. This disables the digital input path to the MCU.

  If the USB module is not used, leave the USB data pins (USB0_DP, USB0_DM) floating. Connect VREGIN and VOUT to ground through a 10 kΩ resistor if the USB module is not used.

5.1.5 Crystal oscillator

This device contains two crystal oscillators, a 26/32 MHz oscillator to support the RF module and a 32 kHz oscillator for the RTC. The outputs of both oscillators are available for use by other modules within the device.

Both oscillators have their own integrated feedback resistor and internal load capacitors as shown in the following figure. The only external components required are the crystals. The load capacitor values for the 26/32 MHz oscillator are adjusted by the ANA_TRIM[BB_XTAL_TRIM] field contained in the RSIM block. The load capacitor values for the RTC oscillator are adjusted by the SCxP bits in the CR register in the RTC module.

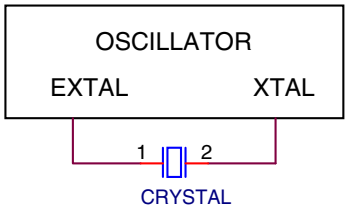


Figure 47. Crystal connection

5.2 Software considerations

All Kinetis MCUs are supported by comprehensive NXP and third-party hardware and software enablement solutions, which can reduce development costs and time to market. Featured software and tools are listed below. Visit http://www.nxp.com/kinetis/sw for more information and supporting collateral.

Evaluation and Prototyping Hardware

- Freedom Development Platform: http://www.nxp.com/freedom

IDEs for Kinetis MCUs

- MCUXpresso IDE: kex.nxp.com
- Partner IDEs: http://www.nxp.com/kide

Development Tools

- PEG Graphics Software: http://www.nxp.com/peg
- MCUXpresso Config Tools: kex.nxp.com)

Run-time Software

- Kinetis SDK: kex.nxp.com or http://www.nxp.com/ksdk
- Kinetis Bootloader: http://www.nxp.com/kboot
- ARM mbed Development Platform: http://www.nxp.com/mbed

For all other partner-developed software and tools, visit http://www.nxp.com/partners.

6 Revision History

The following table provides a revision history for this document.

Table 121. Revision History

Rev. No.	Date	Substantial Changes
1	09/2018	Initial NDA release
1.1	11/2018	• Updated for TBD data.

How to Reach Us:

Home Page:
nxp.com

Web Support:
nxp.com/support

Document Number RV32M1
Revision 1.1, 11/27/2018